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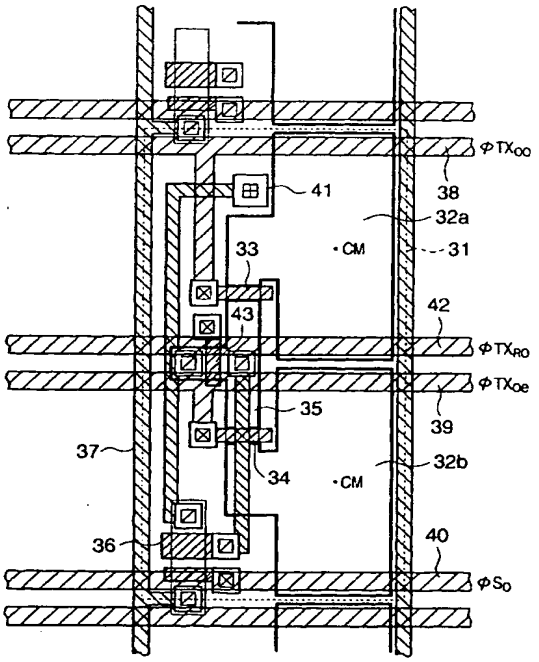
(54) Image sensing apparatus and system including same

(57) In an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, the plurality of photoelectric conversion elements are arranged at a predetermined interval.

FIG. 3



EP 0 954 032 A2

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an image sensing apparatus in which a plurality of pixels share a common circuit and an image sensing system using the apparatus.

[0002] Conventionally, as an image sensing apparatus using a gain cell, or an active pixel sensor (APS), there are image sensing apparatuses utilizing MOS FET, JFET, bipolar transistor.

[0003] These image sensing apparatuses amplify photo-charges generated by photodiodes, that are photoelectric conversion elements, by various methods, then output the amplified photo-charge signals as image information. Since an amplifier for amplifying photo-charge exists in each pixel, the pixel is called a gain cell or an APS.

[0004] An APS includes an amplifier and its controller in each pixel, therefore, the percentage of an area reserved for the photoelectric conversion element in a pixel (area ratio) or area where light incidents in a pixel (aperture) tends to be small. This may cause deterioration of the dynamic range, sensitivity, and the S/N ratio of an image sensing apparatus.

[0005] As described above, when an amplifier is provided in each pixel, as shown in Fig. 40, the aperture decreases. To prevent the decrease in the area or the aperture caused by the amplifier, methods of sharing an amplifier by a plurality of pixels, as disclosed in the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, have been proposed.

[0006] Figs. 41 and 42 illustrate configurations shown in the above documents. Referring to Figs. 41 and 42, reference PD1 to PD4 denote photodiodes as photoelectric conversion elements; M_{TX1} to M_{TX4} are MOS transistors for transferring photo-charges generated by the photodiodes PD1 to PD4; M_{RES} is a MOS transistor for resetting the MOS transistors M_{TX1} to M_{TX4}; and M_{SF} and M_{SEL} are MOS transistors configuring an amplifier (source follower). M_{SEL} also functions as a selection switch for selecting a pixel.

[0007] However, in the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, no practical layout of the foregoing elements on a chip when a plurality of pixels share a single amplifier is discussed.

[0008] Further, there is no description about a layout in a case where an amplifier, shared by a plurality of pixels, is replaced by another unit.

SUMMARY OF THE INVENTION

[0009] The present invention has been made in consideration of the above situation, and has as its first object to provide an image sensing apparatus, in which a common circuit, such as an amplifier, is shared by a plurality of pixels, achieving good performance without deterioration in resolution.

[0010] Further, it is the second object of the present invention to provide an image sensing apparatus having a noise reduction system, preferably used in the image sensing apparatus, in which a common circuit is shared by a plurality of pixels.

[0011] It is the third object of the present invention to provide an image sensing system using the foregoing image sensing apparatuses as a sensor unit.

[0012] According to the present invention, the foregoing first object is attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, wherein the plurality of photoelectric conversion elements are arranged at a predetermined interval.

[0013] The first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in two dimensions, wherein photoelectric conversion elements, out of the plurality of photoelectric conversion elements, which are covered by a color filter that contributes mostly to forming a luminance signal are arranged in a same interval both in the horizontal and vertical directions by arranging adjoining rows or columns of photoelectric conversion elements shifted from each other.

[0014] Further, the first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising adjustment means for adjusting centers of mass of light-receiving areas of the plurality of photoelectric conversion elements provided in a central portion of the image sensing apparatus, so as to be apart at a same spatial interval.

[0015] Furthermore, the first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising adjustment means for adjusting centers of mass of light-receiving areas of photoelectric conversion elements selected from the plurality of photoelectric conversion elements, provided in a central portion of the image sensing apparatus, on the basis of a predetermined condition, so as to be apart at a same spatial interval.

[0016] Further, to achieve the second object of the present invention, noise reading means for reading a noise of the common circuit; first signal reading means for reading a first signal through the common circuit; second signal reading means for reading a second sig-

nal through the common circuit; and noise reduction means for reducing the noise from the first and second signals are further provided.

[0017] Alternatively, noise reading means for reading a noise of the common circuit; signal reading means for reading a plurality of signals through the common circuit; and noise reduction means for reducing the noise from the plurality of signals are further provided.

[0018] Further, the third object of the present invention is achieved by providing an image sensing system having the image sensing apparatus as described above, a lens system for forming an image on the image sensing apparatus, and a signal processing circuit for processing an output signal from the image sensing apparatus.

[0019] Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the Fig. 5res thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Fig. 1 is a block diagram illustrating a configuration of the image sensing system according to an embodiment of the present invention;
Fig. 2A shows a layout of amplifiers in-pixels according to a first embodiment of the present invention;
Fig. 2B shows another layout of amplifiers in pixels according to the first embodiment of the present invention;
Fig. 3 shows a practical pattern layout of two photodiodes and an amplifier according to the first embodiment of the present invention;
Fig. 4 is a brief view of Fig. 3 from which a part of lines are omitted;
Fig. 5 shows another practical pattern layout of two photodiodes and an amplifier according to the first embodiment of the present invention;
Fig. 6 is a brief view of Fig. 5 from which a part of lines are omitted;
Fig. 7 is an enlarged view showing vicinity of a floating diffusion portion according to the first embodiment of the present invention;
Fig. 8 is an enlarged view showing vicinity of the floating diffusion portion according to the first embodiment of the present invention;
Fig. 9 is a circuit diagram of a unit cell of a CMOS sensor in which two photodiodes share one amplifier according to the first embodiment of the present invention;
Fig. 10 is a circuit diagram of the image sensing apparatus including a signal processing circuit according to the first embodiment of the present invention;
Fig. 11 is a timing chart for operating an image sensing apparatus according to the first and second embodiments of the present invention;
Fig. 12 is a timing chart for operating the apparatus according to the first and second embodiments of the present invention;
Fig. 13 shows a layout of common circuits in pixels according to the second embodiment of the present invention;
Fig. 14 shows another layout of common circuits in pixels according to the second embodiment of the present invention;
Fig. 15 is a practical pattern layout of the common circuits each shared by two photodiodes according to the second embodiment of the present invention;
Fig. 16 is a circuit diagram of the image sensing apparatus including a signal processing circuit according to the second embodiment of the present invention;
Fig. 17 is a circuit diagram of a unit cell configured with a common circuit and photodiodes according to the second embodiment of the present invention;
Fig. 18 is an explanatory view for explaining a signal processing circuit;
Fig. 19 is a layout of amplifiers in pixels according to a third embodiment of the present invention;
Fig. 20 is another layout of amplifiers in pixels according to the third embodiment of the present invention;
Fig. 21 is another layout of amplifiers in pixels according to the third embodiment of the present invention;
Fig. 22 is another layout of amplifiers in pixels according to the third embodiment of the present invention;
Fig. 23 is a practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;
Fig. 24 is another practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;
Fig. 25 is an explanatory view for explaining a variation of a layout;
Fig. 26 shows a practical pattern layout according to the third embodiment of the present invention;
Fig. 27 shows another layout of light-receiving areas according to the third embodiment of the present invention;
Fig. 28 shows another practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;
Fig. 29 is an example when on-chip lens according to the third embodiment of the present invention;
Fig. 30 is a circuit diagram of a unit cell of a CMOS sensor having the aforesaid configurations accord-

ing to the third embodiment of the present invention;
Fig. 31 is a circuit diagram of the image sensing apparatus including a signal processing unit according to the third embodiment of the present invention;
Fig. 32 is a timing chart for operating an image sensing apparatus according to the third embodiment of the present invention;
Fig. 33 is a circuit diagram of an image sensing apparatus including the signal processing unit according to a first modification of the third embodiment of the present invention;
Fig. 34 is a circuit diagram of an image sensing apparatus including a signal processing unit according to a second modification of the third embodiment of the present invention;
Fig. 35 is a timing chart for operating the image sensing apparatus shown in Fig. 34 according to the second modification of the third embodiment of the present invention;
Fig. 36 is a timing chart during a vertical blanking period according to the second configuration of the third embodiment of the present invention;
Fig. 37 shows a configuration of a common circuit according to a fourth embodiment of the present invention;
Fig. 38 is a circuit diagram of a unit cell of another image sensor to which the present invention is applied;
Fig. 39 is a circuit diagram of a configuration of an amplifier shared by four photodiodes according to an embodiment of the present invention;
Fig. 40 shows a conventional layout of amplifiers in pixels;
Fig. 41 is a circuit diagram of a conventional configuration;
Fig. 42 is a circuit diagram of another conventional configuration;
Fig. 43 shows a layout of common circuits in pixels when each common circuit is shared by two pixels;
Fig. 44 shows a practical pattern layout of two photodiodes and an amplifier shown in Fig. 43;
Figs. 45A and 45B shows color filter arrangements;
Fig. 46 is a layout of common circuits in pixels when each common circuit is shared by four pixels; and
Fig. 47 shows a practical pattern layout of four photodiodes and an amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Preferred embodiments of the present invention will be described in detail below in accordance with the accompanying drawings.

<Possible Arrangements of Pixels and Common Circuit>

[0022] First, possible arrangements of a plurality of pixels and a common circuit, shared by the pixels, based on the disclosure of the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, are described below. In the following explanation, an amplifier is used as an example of the common circuit in an image sensing apparatus.

[0023] Fig. 43 shows an example of a layout of common circuits in pixels, when each common circuit is shared by two pixels. In Fig. 43, a case where each amplifier, as the common circuit, is shared by two pixels in two rows is shown, and, more specifically, each amplifier 204 is arranged between two photodiodes 203 above and below the row of the amplifiers 204 (such as, pairs of photodiodes a_{11} and a_{21}, a_{12} and a_{22}, a_{31} and a_{41}, a_{32} and a_{42}, and so on). Note, a photodiode 203, which is a photoelectric conversion element, and one half of the amplifier 204 configure a pixel. Reference numeral 201 indicates a unit cell repeated in the column direction, and reference numeral 202 indicates the unit cell repeated in the row direction.

[0024] Fig. 44 shows a practical pattern layout of two photodiodes and an amplifier (a signal unit cell). The image sensing apparatus is a CMOS sensor, in this case.

[0025] Referring to Fig. 44, reference numeral 221 denotes the unit cell (area surrounded by a dash line), which are referred to by reference numerals 201 and 202 in Fig. 43, having a size of two pixels, and repeatedly arranged in both the row and column directions. Light incidents on photodiodes 222a and 222b (areas surrounded by bold lines, correspond to the photodiode pairs a_{11} and a_{21}, a_{12} and a_{22}, a_{31} and a_{41}, a_{32} and a_{42}, and so on, shown in Fig. 43) is converted into electrical charges (photo-charges), and accumulated within the photodiodes 222a and 222b. The accumulated photo-charges are respectively transferred to a floating diffusion portion 225 (also surrounded by a bold line) via a transfer gate 223 for an odd row and a transfer gate 224 for an even row, further transferred to the gate (floating gate) 226 of a MOS-type amplifier, which is the amplifier 204. Current flowing through the MOS-type amplifier is modulated, and the output current is taken out from the pixel array via a vertical signal line 227.

[0026] X-Y addressing of the two dimensional pixel array, as shown in Fig. 43, in the image sensing apparatus is realized by the vertical signal line 227, an odd-row scanning line 228, an even-row scanning line 229, and a row selection line 230. In addition, a power line 231 for supplying electric power V_{DD} and a reset line 232 for resetting the floating diffusion portion 225 and the gate 226 to a predetermined voltage are also arranged in the horizontal direction.

[0027] The lines 228 to 232 are arranged above the wiring of the unit cells, and the lines are basically wide. The area under these five opaque lines 228 to 232 does not receive light, therefore, the amplifier 204 is arranged under the lines 228 to 232. For the above reason, the two photodiodes sharing the amplifier are considered to be arranged on the upper and lower sides of the ampli-

fier.

[0028] With this layout, however, since the centers of mass (CM) of the photodiodes are not equal, as seen in Fig. 43, the following problems arise.

[0029] First, if the pixel array outputs signals of a single color, since spatial frequency and resolution are different in one part from the other, the resolution deteriorates, and moreover, moiré appears.

[0030] It is possible to cover the pixel array with a color filter whose color arrangement is as shown in Fig. 45A or 45B. In designing the color filter, colors may be arranged so that difference between intervals between pixels corresponding to each color is minimized. In this case, however, the color arrangement is strictly limited.

[0031] Further, if the Bayer filter as shown in Fig. 45A is used, intervals between pixels corresponding to green (G) filter, which contributes most to luminance (Y) signals that the human eye is most sensitive to, are not equal. More specifically, considering the positions of the photodiodes, e.g., a_{12}, a_{23}, and a_{32} corresponding to the green filter, the distance between the photodiodes a_{12} and a_{23} in the column direction is different from the distance between the photodiodes a_{23} and a_{32} in the column direction. Thus, the filter arrangement causes different intervals between pixels corresponding to green filter, resulting in a moiré problem; therefore, the quality of an obtained image is not good.

[0032] Next, referring to Fig. 46, an example of a layout of common circuits in pixels when each common circuit is shared by four pixels, is explained.

[0033] In this case, an amplifier, i.e., the common circuit, is shared by adjoining four pixels in two rows and two columns (2 × 2), and each amplifier 174 is surrounded by four photodiodes 173 (such as 2 × 2 photodiodes b_{11}, b_{12}, b_{21}, and b_{22}, and b_{31}, b_{32}, b_{41}, and b_{42}). In Fig. 46, reference numeral 171 indicates a unit cell repeated in the column direction, and reference numeral 172 indicates the unit cell repeated in the row direction.

[0034] Fig. 47 shows a practical pattern layout of four photodiodes and an amplifier. The image sensing apparatus is a CMOS sensor in this case, too.

[0035] Referring to Fig. 47, reference numeral 181 denotes the unit cell (area surrounded by a dash line), which is referred to by reference numerals 171 and 172 in Fig. 46, having a size of four pixels, and repeatedly arranged in both the row and column directions. Light incidents on photodiodes 182a to 182d (correspond to either one of groups of the photodiodes, b_{11}, b_{12}, b_{21}, and b_{22}, and b_{31}, b_{32}, b_{41}, and b_{42} shown in Fig. 46) is converted into electrical charges (photo-charges), and accumulated within the photodiodes 182a to 182d. The accumulated charges are respectively transferred to a floating diffusion portion 185 via transfer gates 183a to 183d, respectively, further transferred to the gate 186 of a MOS-type amplifier, which is the amplifier 174. Current flowing through the MOS-type amplifier is modulated, and the output current is taken out from the pixel array via a vertical signal line 187.

[0036] X-Y addressing of the two dimensional pixel array, as shown in Fig. 46, in the image sensing apparatus is realized by the vertical signal line 187, scanning lines 188a to 188d, and a row selection line 190. In addition, a power line 191 for supplying electric power V_{DD} is arranged in the column direction, and a reset line 192 for resetting the floating diffusion portion 185 and the gate 186 to a predetermined voltage are arranged in the horizontal direction.

[0037] The lines 188 to 192 are arranged above the wiring of the unit cells, and the lines are basically wide. The area under these six opaque lines 188 to 192 does not receive light, therefore, the amplifier 174 is arranged under the lines 188 to 182. For the above reason, the four photodiodes sharing the amplifier are considered to be arranged around the amplifier.

[0038] With this layout, however, since the intervals between the centers of mass (CM) of photodiodes are not equal, as seen in Fig. 46, the following problem arises.

[0039] If the pixel array outputs signals of a single color, since spatial frequency and resolution are different in one part from another, the resolution deteriorates, and moreover, moiré appears. The moiré is a serious problem, and an image sensing apparatus with a moiré problem does not sell on the market. This can be said for any image sensing apparatus having a configuration in which any number of pixels share a single common circuit.

[0040] Accordingly, the inventors of the present application have developed image sensing apparatuses having improved arrangements of pixels and circuits shared by a plurality of pixels.

[0041] The image sensing apparatuses will be described below in detail.

<Basic Configuration of Image Sensing Apparatus>

[0042] Fig. 1 is a block diagram illustrating a configuration of the image sensing apparatus according to an embodiment of the present invention.

[0043] As shown in Fig. 1, light incoming through an optical system 21 forms an optical image on a CMOS sensor 22, and converted into electric charges by a pixel array arranged on the CMOS sensor. The photo-charges are further converted, processed and outputted by a signal processing circuit 23 in a predetermined method. The processed signals are recorded on an information storage medium or outputted by a. recording/transmission system 24. The recorded or transmitted information is retrieved by a retrieving system 27. The CMOS sensor 22 and the signal processing circuit 23 are controlled by a timing controller 25, and the optical system 21, the timing controller 25, the recording/transmission system 24, and the retrieving system 27 are controlled by a system controller 26.

[0044] Next, the CMOS sensor 22 according to the present invention will be described in detail.

<First Embodiment>

[0045] Fig. 2A shows a layout of amplifiers 12 in pixels when each amplifier 12 is shared by two pixels adjoining in the column direction, and Fig. 2B shows a layout of amplifiers 12 in pixels when each amplifier 12 is shared by two pixels adjoining in the row direction.

[0046] In Fig. 2A, two photoelectric conversion elements 11 (such as, pairs of the elements p_{11} and p_{21}, p_{31} and p_{41}, p_{12} and p_{22}, p_{32} and p_{42}, and so on) sharing one amplifier 12 are arranged next to each other in the column direction, and the amplifier 12 is arranged along the adjoining pixels. In this manner, intervals between the centers of mass of the photoelectric conversion elements 11 (e.g., p_{11}, p_{21}, p_{31}, p_{41}, p_{12}, p_{22}, p_{32}, p_{42}) in both the row and column directions become equal. Reference numeral 13 indicates a unit cell repeated in.the column direction, and reference numeral 14 indicates the unit cell repeated in the row direction.

[0047] Further, in Fig. 2B, two photoelectric conversion elements 11 (such as, pairs of the elements p_{11} and p_{12}, p_{13} and p_{14}, p_{21} and p_{22}, p_{23} and p_{24}, p_{31} and p_{32}, p_{33} and p_{34}, and so on) sharing one amplifier 12 are arranged next to each other in the row direction, and the amplifier 12 is arranged along the adjoining pixels. In this manner, intervals between the centers of mass of the photoelectric conversion elements 11 (p_{11}, p_{12}, p_{13}, p_{14}, p_{21}, p_{22}, p_{23}, p_{24}, p_{31}, p_{32}, p_{33}, p_{34}) in both the row and column directions also become equal. Reference numeral 15 indicates a unit cell repeated in the column direction, and reference numeral 16 indicates the unit cell repeated in the row direction.

[0048] In the first embodiment, the number, N, of photoelectric conversion elements 11 sharing each amplifier 12 is two (N = 2), however, the number N may be an arbitrary number greater than 2.

[Layout 1]

[0049] Fig. 3 shows a practical pattern layout of two photodiodes and an amplifier in the CMOS sensor 22, and Fig. 4 is a brief view of Fig. 3 from which a part of lines are omitted.

[0050] The CMOS sensor, as shown in Fig. 3, is formed on a singlecrystalline silicon substrate based on a layout rule 0.4μm. Each pixel is a square, 8μm each side, and a source follower amplifier, as the amplifier 12, is shared by two adjoining pixels arranged in the column direction. Therefore, the size of a unit cell 31, shown by a dash line and is referred to by reference numerals 13 and 14 in Fig. 2A, is 8μm × 16μm. A plurality of unit cells 31 are arranged in two dimensions.

[0051] The photodiodes 32a and 32b, i.e., the photoelectric conversion elements, are formed on the right portion of respective pixels, and the shapes of the photodiodes 32a and 32b are almost mirror images. Further, the photodiodes 32a and 32b are designed so that the center of masses (CM) of light-receiving areas of the photodiodes 32a and 32b are located at a substantially identical position of each pixel. In Fig. 3, the areas of the photodiodes 32a and 32b, and the area of a floating diffusion (FD) portion 35 are shown by bold lines. Further, in Fig. 3, reference numeral 38 denotes an odd-row scanning line for controlling each transfer gate 33 in an odd-number row; 39, an even-row scanning line for controlling each transfer gate 34 in an even-number row; 40, a row selection line; and 42, a reset line for controlling the gate 43 of a MOS transistor. In Fig. 4, the lines 38 to 42 are not shown.

[0052] Photo-charges accumulated in the photodiodes 32a and 32b are transferred to the FD portion 35 via the transfer gate 33 for the odd-number row and the transfer gate 34 for the even-number row. The size of the both transfer gates 33 and 34 is L = 0.4μm, W = 1.0μm (L is a channel length and W is a channel width). The FD portion 35 is connected to the gate 36 of a source follower via an aluminum (A1) wire having a width of 0.4μm, and the photo-charge transferred to the FD portion 35 modulates the gate voltage of the gate 36. The size of the MOS transistor of the gate 36 is L = 0.8μm, W = 1.0μm, and the total capacitance of the FD portion 35 and the gate 36 is about 5fF. Since Q = CV, the gate voltage of the gate 36 changes by 3.2 volts in response to the transference of 10^5 electrons.

[0053] Current flowing in from a V_{DD} terminal 41 is modulated by the MOS transistor of the gate 36, and transferred to a vertical signal line 37. Current flowing through the vertical signal line 37 is processed by a signal processing circuit (not shown) and formed into image information.

[0054] Thereafter, in order to set the potentials of the photodiodes 32a and 32b, the FD portion 35, and the gate 36 to the predetermined potential V_{DD}, the gate 43 of the MOS transistor connected to the reset line 42 is opened (at this time, the transfer gate 33 for the odd-number row and the transfer gate 34 for the even-number row are also opened), thereby the photodiodes 32a and 32b, the FD portion 35, and the gate 36 are electrically connected to the V_{DD} terminal 41.

[0055] Thereafter, the transfer gates 35 and 36 are closed, thereby the accumulation of photo-charges in the photodiodes 32a and 32b start again.

[0056] The total number of the lines arranged in each unit cell in the horizontal direction is four, specifically, the odd-row scanning line 38, the even-row scanning line 39, the row selection line 40, and the reset line 42. The four lines are arranged in such a manner that two lines each are arranged on the upper and lower ends of each pixel, as shown in Fig. 3.

[0057] Since these lines are thick wires and provided over pixels, as described above, an increase in the number of lines results in an increase in area which can not receive light, which reduces aperture. Further, if the number of lines provided over a row is different from the number of lines arranged over another row, such that two lines in one row and three lines in the other row, the

apertures and the centers of mass of photodiodes adjoining in the column direction become different in one row from the other.

[0058] In layout 1, the power supply voltage V_{DD} is provided to every pixel by connecting a power supply (not shown) with each pixel via a metal light-shield layer (not shown), arranged on the top layer of the CMOS sensor, and the V_{DD} terminal 41, formed as a through hole, in order to avoid the problem described in the previous paragraph.

[0059] With the layout 1 as described above, it is possible to provide a CMOS sensor having a plurality of pixels, arranged in the same interval from each other, which have relatively high area ratio or high aperture.

[0060] It should be noted that the area ratio or aperture may be further increased by using known on-chip convex lenses, for instance.

[0061] Further, the metal layer used for supplying the power supply voltage VDD is not limited to a light-shield film, and may be an electrode material used for forming capacitor, for instance, placed over the entire pixel.

[Layout 2]

[0062] Fig. 5 shows another practical pattern layout of two photodiodes and an amplifier in the CMOS sensor 22, and Fig. 6 is a brief view of Fig. 5 from which several lines are omitted. Further, Figs. 7 and 8 are enlarged views showing vicinity of an FD portion. Specifically, Fig. 7 is a view when a wire over a gate 54 is omitted, and Fig. 8 is a view when a wire is provided over the gate 54.

[0063] Referring to Fig. 6 to 8, the areas of photodiodes 52a and 52b, and an FD portion 55 are shown by bold lines. The layout 2 also shows a case where two adjoining pixels share a single amplifier, similarly to the layout 1, but the two adjoining pixels are arranged in the row direction. The centers of mass of the two adjoining photodiodes are located at a substantially same position of the each photodiode.

[0064] Referring to Figs. 5 and 6, reference numerals 52a and 52b are the photodiodes; 53, a transfer gate for an odd-number column; 54, a transfer gate for an even-number column; 55, the FD portion; 56, the gate of a source follower; 57, a vertical signal line; 58, an odd-column scanning line for controlling the transfer gate 53 in an odd-number column; 59, an even-column scanning line for controlling the transfer gate 54 in an even-number column; 60, a row selection line; and 62, a reset line for controlling the gate 63 of a MOS transistor. Note, a wire connecting the gate 56 of the source follower and the FD portion 55 crosses over the gate 54 as shown in Fig. 8.

[0065] In layout 2, the area ratio or the aperture is improved comparing to the layout 1 in which sharing an amplifier with two pixels adjoining in the column direction. Accordingly, a CMOS sensor of wide dynamic range, high sensitivity, and high S/N ratio is realized.

[0066] In layout 2, necessary four lines are arranged, and a power supply line 61 for providing a voltage V_{DD} is arranged in the column direction on the side of photodiodes opposite to the side of the vertical signal line 57.

[Noise Reduction]

[0067] The inventors of the present application also have developed a signal read circuit, for reducing noise, suitably used in an image sensing apparatus having a configuration, as described above, in which a plurality of pixels share an amplifier.

[0068] The noise reduction operation is explained with reference to Figs. 9 and 10.

[0069] Fig. 9 shows a circuit configuration of a unit cell of a CMOS sensor in which two photoelectric conversion elements share one amplifier. Referring to Fig. 9, PD1 and PD2 denote photodiodes as photoelectric conversion elements; M_{TX1} and M_{TX2}, MOS transistors for transferring photo-charges accumulated in the photodiodes PD1 and PD2 to an FD portion; M_{RES}, a MOS transistor for resetting the FD portion; and M_{SF} and M_{SEL}, MOS transistors configuring a source follower. The MOS transistor M_{SEL} also functions as a selection switch for selecting a photodiode.

[0070] First, reset operation is performed by turning on the MOS transistor M_{RES}, then, noise signal is. read out from the MOS transistors M_{SF} and M_{SEL} configuring the source follower. Next, photo-charge accumulated in the photodiode PD1 is transferred to the gate of the MOS transistor M_{SF} via the MOS transistor M_{TX1}, then read out as a first signal via the MOS transistors M_{SF} and M_{SEL}. Thereafter, reset operation is performed again, and photo-charge accumulated in the photodiode PD2 is transferred to the gate of the MOS transistor M_{SF} via the MOS transistor M_{TX2}, then read out as a second signal via the MOS transistors M_{SF} and M_{SEL}. Accordingly, the noise signal, the first signal, and the second signal are obtained, and, by subtracting the noise signal from the first and second signals, a signal corresponding to the photodiode PD1 without the noise component as well as a signal corresponding the photodiode PD2 without the noise component are obtained

[0071] Further, it is possible to add the photo-charge signal corresponding to the photodiode PD1 and the photo-charge signal corresponding to the photodiode PD2 by transferring photo-charge accumulated in the photodiode PD2 to the gate of the MOS transistor M_{SF} while photo-charge accumulated in the photodiode PD1 is kept at the gate of the MOS transistor M_{SF} by changing operation timing.

[0072] Next, the image sensing apparatus including a signal processing circuit according to the first embodiment will be explained below. Fig. 10 shows an equivalent circuit of the image sensing apparatus including the signal processing circuit according to the first embodiment, and Figs. 11 and 12 are timing charts for operating the apparatus.

[0073] Referring to Figs. 10 and 11, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal ϕTX_{R0-1} which is applied to the reset line 62 of the first row is activated during a horizontal blanking period (i.e., when a signal ϕHBL is high), and signals ϕTX_{R0-i} (i is a row number. Below, the last part of the subscript, -i, is omitted.) for subsequent lines are activated in the same manner. Accordingly, all the pixels in every row are reset to the reset potential V_{DD}.

[0074] In each horizontal blanking period, during a period T_1, a signal ϕL becomes high and a transistor 81, connected to the vertical signal line 57, is turned on and the vertical signal line 57 is reset. Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors 82-1, 82-2, and 82-3 are turned on. Accordingly the upstream part of transistors for reading signals, 84-1, 84-2, and 84-3, and capacitors 83-1, 83-2, and 83-3 (C_{TN}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line 57, and reset. Accordingly, residual charges in the capacitors 83-1, 83-2, and 83-3, for instance, are removed.

[0075] Thereafter, in a period T_2, the signal ϕTX_{RO} to be applied to the reset line 62 is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors M_{SF} and M_{SEL} in each unit cell, is reset to the voltage V_{DD}.

[0076] Then, in a period T_3, a signal ϕRV becomes high and a transistor 80 for grounding, connected to the vertical signal line 57, is turned on, and the vertical signal line 57 is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor 83-1 (C_{TN}) for storing a noise component to the vertical signal line 57, and the transistor 82-1 is turned on. At this time, a signal ϕS_O to be applied to the row selection line 60 is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor M_{SF} flows from the V_{DD} terminal 41 to the capacitor 83-1 (C_{TN}), thereby the capacitor 83-1 (C_{TN}) stores charge corresponding to the noise component.

[0077] Next, in a period T_4, a signal ϕTX_{OO} applied to the odd-column scanning line 58 is changed to high, in turn, the transfer gate (MOS transistor M_{TX1}, in this case) in an odd-number column is turned on, and photo-charge accumulated in the photodiode PD1 is transferred to the floating gate of the MOS transistor M_{SF}. The capacitor 83-1 (C_{TN}) for storing the noise component is disconnected from the vertical signal line 57 when the signal ϕT_N becomes low, and the capacitor 83-2 (C_{TS1}) for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the photodiode PD1, for instance, in an odd-number column is stored in the capacitor 83-2 (C_{TS1}) via the vertical signal line 57.

[0078] Next, in a period T_5, the signal ϕL becomes high, and only the vertical signal line 57 is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1}, and ϕT_{S2}, are low, other portions are not reset, and their states are preserved.

[0079] Next, the signal ϕTX_{RO} applied to the reset line 62 is changed to high between periods T_5 and T_6, and the gate of the source follower amplifier (i.e., the gate of MOS transistor M_{SF}) is reset to the potential V_{DD}.

[0080] In the period T_6, a signal ϕTX_{Oe} applied to the even-column scanning line 59 is changed to high, and photo-charge accumulated in the photodiode PD2 in an even-number column is transferred to the floating gate of the MOS transistor M_{SF}. At this time, the signal ϕT_{S2} is changed to high, thus the capacitor 83-3 (C_{TS2}) for storing another photo-charge signal is electrically connected to the vertical signal line 57, and photo-charge accumulated in the photodiode PD2, for instance, in an even-number column is stored in the capacitor 83-3 (C_{TS2}) via the vertical signal line 57.

[0081] In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors 83-1, 83-2, and 83-3 (C_{TN} C_{TS1}, C_{TS2}) by each column for a row.

[0082] Next, in a period T_7, in order to sequentially transfer the charges stored in the capacitors 83-1, 83-2, and 83-3 (C_{TN} C_{TS1}, C_{TS2}) to amplifiers 86-1 to 86-3, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register 71, and transistors 84-1 to 84-3, provided for each column, are turned on; thereby the capacitors 83-1 to 83-3 (C_{TN} C_{TS1}, C_{TS2}) are connected to the respective amplifiers 86-1 to 86-3. From the capacitors 83-1 to 83-3 (C_{TN} C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier 87-1, a signal S1 obtained by subtracting the noise component from the first signal is outputted, and a signal S2 obtained by subtracting the noise component from the second signal is outputted from a differential amplifier 87-2. Note that accumulation of photo-charges in the photodiodes is also performed during the period T_7.

[0083] In a case where the signal ϕTX_{RO} to be applied to the reset line 62 between the period T_5 and the period T_6 is not changed to high and reset operation is not performed, photo-charge generated by the photodiode PD2 in an even-number column is transferred to the floating gate of the MOS transistor M_{SF} where photo-charge generated by the photodiode PD1 remains; accordingly, a signal of the photodiode PD1 in the odd-number column and a signal of the photodiode PD2 in the even-number row are stored in the capacitor 83-3 (C_{TS2}) via the vertical signal line 57. Therefore, a noise component, a signal corresponding to one photodiode (single signal component), and a signal corresponding to two photodiodes (double signal component) are stored in the capacitors 83-1 to 83-3 (C_{TN}, C_{TS1}, C_{TS2}). Then, the noise component, the single signal component, and the double signal component are outputted to the amplifiers 86-1 to 86-3 during the period T_7. Thereafter, the noise component is subtracted from the single signal component by the differential amplifier 87-1 and a signal S1 is

outputted. Similarly, the noise component is subtracted from the double signal component by the differential amplifier 87-2 and a signal S2 is outputted.

[0084] Further, the first embodiment of the present invention is not limited to two-dimensional array, and capable of applying to an one-dimensional line sensor.

[0085] According to the first embodiment as described above, it is possible to realize a high precision image sensor without causing deterioration of performance, such as deterioration of resolution and generation of moiré, for instance. In addition, yield of image sensing apparatus becomes high.

<Second Embodiment>

[0086] Next, the second embodiment of the present invention will be explained.

[0087] Figs. 13 and 14 show other layouts of amplifiers 12, as common circuits, and photodiodes 11 when each amplifier 12 is shared by two photodiodes 11.

[0088] As shown in Fig. 13, the photodiodes 11 are arranged so that adjoining rows are shifted from each other by one half pitch. In odd-number rows, pixels covered by green (G) filter (referred to as "G pixel" hereinafter), which contribute mainly to a luminance (Y) signal, are respectively set across the amplifiers from pixels covered by red (R) filter (referred to as "R pixel" hereinafter), which contribute to a color-difference signal, and in even-number rows, G pixels are respectively set across the amplifiers from pixels covered by blue (B) filter (referred to as "B pixel" hereinafter), which also contributes to a color-difference signal. By arranging the G pixels in adjoining rows, shifted by one and half pitches in the row direction, intervals between G pixels in the row direction becomes the same, further, intervals between the G pixels in the column direction also become the same. Accordingly problem of moiré is solved, and a sensed image does not look deteriorated.

[0089] Further, Fig. 14 shows an example when photodiodes 11 are arranged so that adjoining columns are shifted from each other by one half pitch.

[0090] Next, Fig. 15 shows a practical pattern layout of two photodiodes and an amplifier, as the common circuit, shared by the two photodiodes 11 arranged on right and left sides of the amplifier 12, as shown in Fig. 13.

[0091] The CMOS sensor, as shown in Fig. 15, is formed on a singlecrystalline silicon substrate. Each pixel is a square, 8μm each side, shown by a dash line 341. As described above, plural pairs of photodiodes are arranged in a two-dimensional array. Between each pair of two photodiodes, the common circuit is arranged. A photodiode covered by G filter (G photodiode) is set on the left side of the common circuit, and a photodiode covered by R or B filter (R/B photodiode) is set on the right side of the common circuit. In Fig. 15, an amplifier, using MOS transistors, is used as the common circuit, as an example. The layout rule is 0.4μm, and an area, area ratio, an aperture area, and aperture ratio of a photodiode 342 as a photoelectric conversion element is 57.96μm^2, 60.4%, 28.88μm^2 and 30.1%, respectively. These figures are very high comparing to conventional figures.

[0092] Reference numeral 343 denotes a transfer gate for transferring photo-charge from a G photodiode 342 to a floating diffusion (FD) portion 345 and reference numeral 344 denotes a transfer gate for transferring photo-charge from an R/B photodiodes 342' also to the FD portion 345. The transfer gates 343 and 344 are MOS transistors, and the channel length and the channel width of each MOS transistor is 0.4μm and 1.0μm, respectively. Reference numeral 347 denotes a reset gate for resetting the FD portion 345 to a potential of a power supply voltage V_{DD} through a terminal 350, and reference numeral 346 denotes a gate of a MOS-type source follower amplifier. The potential of the gate 346 changes depending upon the transferred charge, and the amplifier modulates current flowing in from the V_{DD} terminal 350.

[0093] The total capacitance of the FD portion 345 and the gate 346 is about 10fF, and as the area of the photodiodes increases, the capacitance also increases. The modulated current is eventually outputted to a vertical signal line 349 via a selection gate 348 for selectively outputting the current.

[0094] Further, reference numerals 351 to 354 denote scanning lines for applying a predetermined potential to the selection gate 348, the transfer gates 343 and 344, and the reset gate 347, respectively.

[Noise Reduction]

[0095] Next, signal processing for reducing noise preferably used in the above-described image sensor is explained.

[0096] Fig. 16 is an equivalent circuit diagram according to the second embodiment. In Fig. 16, the same units and elements as those shown in Figs. 10 and 15 are referred to by the same reference numerals. Further, Fig. 17 is an equivalent circuit diagram of a unit cell 374, surrounded by a dash line in Fig. 16 and whose pattern layout is shown in Fig. 15, configured with a common circuit 372 and photodiodes arranged on the both sides of the common circuit 372.

[0097] In Fig. 17, reference numeral 350 is the V_{DD} terminal; 345, the FD portion; 363, a reset unit, such as a MOS transistor (reset MOS), for resetting the FD portion 345; 364 and 364', transfer units, such as MOS transistors (transfer MOS), for transferring photo-charges from the photodiodes 342 and 342' to the FD portion 345; 365, an amplifier, such as a MOS transistor, for amplifying the change in the potential at the FD portion 345; and 366, a MOS transistor for selection (selection MOS) for selectively outputting a signal from the amplifier 365 to the vertical signal line 349. Further, the scanning lines 354, 351, 352 and 353 are for applying potentials for turning on or off the reset MOS 363, the selection MOS

366, the transfer MOS 364, and the transfer MOS 364', respectively. In the unit cell 374, the MOS transistors 363, 364, 364', 365, and 366 configure the common circuit. Further, in the pattern layout shown in Fig. 15, the transfer gate 343 corresponds to the gate of the transfer MOS 364 of Fig. 17, the transfer gate 344 corresponds to the gate of the transfer MOS 364', the reset gate 347 corresponds to the gate of the reset MOS 363, and the selection gate 348 corresponds to the gate of the selection MOS 366.

[0098] Next, referring to the circuit diagrams shown in Figs. 16 and 17, and timing charts shown in Figs. 11 and 12, the noise reduction operation is explained.

[0099] Referring to Fig. 11, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal ϕTX_{R0-1} which is applied to the reset line 354 of the first row is activated during a horizontal blanking period (i.e., when a signal ϕHBL is high), and signals ϕTX_{R0-i} (i is a row number. Below, the last part of the subscript, -i, is omitted.) for subsequent lines are applied in the same manner. Accordingly, all the pixels in every row are reset to the reset potential. V_{DD}.

[0100] In each horizontal blanking period, during a period T_1, a signal ϕL becomes high, as shown in Fig. 12, and a transistor 81, connected to the vertical signal line 349, is turned on and the vertical signal line 349 is reset. Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors 82-1, 82-2, and 82-3 are turned on. Accordingly wires in the upstream of transistors for reading signals, 84-1, 84-2, and 84-3, and capacitors 83-1, 83-2, and 83-3 (C_{TN}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line 349, and reset. Accordingly, residual charge in the capacitors 83-1, 83-2, and 83-3, for instance, are removed.

[0101] Thereafter, in a period T_2, the signal ϕTX_{RO} to be applied to the reset line 354 is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors 365 and 366 in each unit cell is reset to the voltage V_{DD}.

[0102] Then, in a period T_3, a signal ϕRV becomes high and a transistor 80 for grounding, connected to the vertical signal line 349, is turned on, and the vertical signal line 349 is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor 83-1 (C_{TN}) for storing a noise component to the vertical signal line 349, and the transistor 82-1 is turned on. At this time, a signal ϕS_O to be applied to the row selection line 351 is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor 365 flows from the V_{DD} terminal 350 to the capacitor 83-1 (C_{TN}), thereby the capacitor 83-1 (C_{TN}) stores charge corresponding to the noise component.

[0103] Next, in a period T_4, a signal ϕTX_{OO} applied to the G pixel scanning line 353 is changed to high, in turn, transfer gate (MOS transistor 364) for the G pixel is turned on, and photo-charge accumulated in the photodiode 342 is transferred to the floating gate of the MOS transistor 365. The capacitor 83-1 (C_{TN}) for storing the noise component is disconnected from the vertical signal line 349 when the signal ϕT_N becomes low, and the capacitor 83-2 (C_{TS1}) for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the G photodiode 342, for instance, is stored in the capacitor 83-2 (C_{TS1}) via the vertical signal line 349.

[0104] Next, in a period T_5, the signal ϕL becomes high, and only the vertical signal line 349 is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1}, and ϕT_{S2}, are low, other portions are not reset, and their states are preserved.

[0105] Next, the signal ϕTX_{RO} applied to the reset line 354 is changed to high between periods T_5 and T_6, and the FD portion 345 is reset to the potential V_{DD}.

[0106] In the period T_6, a signal ϕTX_{Oe} applied to the R/B pixel scanning line 352 is changed to high, and photo-charge accumulated in the R/B photodiode 342' is transferred to the floating gate of the MOS transistor 365. At this time, the signal ϕT_{S2} is changed to high, thus the capacitor 83-3 (C_{TS2}) for storing another photo-charge signal is electrically connected to the vertical signal line 349, and charge accumulated in the R/B photodiodes 342', for instance, is stored in the capacitor 83-3 (C_{TS2}) via the vertical signal line 349.

[0107] In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors 83-1, 83-2, and 83-3 (C_{TN}, C_{TS1}, C_{TS2}) by each column for a row.

[0108] Next, in a period T_7, in order to sequentially transfer the charges stored in the capacitors 83-1, 83-2, and 83-3 (C_{TN}, C_{TS1}, C_{TS2}) to amplifiers 86-1 to 86-3, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register 71, and transistors 84-1 to 84-3, provided for each column, are turned on; thereby the capacitors 83-1 to 83-3 (C_{TN}, C_{TS1}, C_{TS2}) are connected to the amplifiers 86-1 to 86-3. From the capacitors 83-1 to 83-3 (C_{TN}, C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier 87-1, a G component signal obtained by subtracting the noise component from the first signal is outputted, and an R/B component signal obtained by subtracting the noise component from the second signal is outputted from a differential amplifier 87-2. Note that accumulation of photo-charges in the photodiodes is also performed during the period T_7.

[0109] In a case where the signal ϕTX_{RO} to be applied to the reset line 354 between the period T_5 and the period T_6 is not changed high and reset operation is not performed, photo-charge generated by the R/B photodiodes 342' is transferred to the floating gate of the MOS transistor 365 where photo-charge generated by the G photodiode 342 remains; accordingly, a signal of the G photodiode 342 and a signal of the R/B photodiode 342' are stored in the capacitor 83-3 (C_{TS2}) via the vertical signal line 349. Therefore, a noise component, a signal

corresponding to one photodiode (single signal component), and a signal corresponding to two photodiodes (double signal component) are stored in the capacitors 83-1 to 83-3 (C_{TN}, C_{TS1}, C_{TS2}). Then, the noise component, the single signal component, and the double signal component are outputted to the amplifiers 86-1 to 86-3 during the period T_7. Thereafter, the noise component is subtracted from the single signal component by the differential amplifier 87-1 and a G component signal is outputted. Similarly, the noise component is subtracted from the double signal component by the differential amplifier 87-2 and a G+R/B component signal is outputted.

[0110] The signal processing circuit 23, shown in Fig. 1, according to the second embodiment is explained with reference to Fig. 18.

[0111] The G and R/B component signals output from the CMOS sensor 22 are converted into luminance (Y) signals and color difference (C_R, C_B) signals. Note that low frequency component of the luminance signals are generated using R, G, and B signals of at least two adjoining rows.

[0112] Further, high frequency component of the luminance signals are generated using high frequency component of G signals in at least two adjoining rows. Accordingly, an image of high resolution and good color reproduction is obtained.

[0113] According to the second embodiment as described above, it is possible to obtain an image sensing apparatus of good sensitivity, high resolution, and wide dynamic range.

<Third Embodiment>

[0114] Next, the third embodiment of the present invention will be explained with reference to accompanying drawings.

[0115] Fig. 19 shows a layout of amplifiers 12 in pixels when each amplifier 12 is shared by four (2 rows × 2 columns) pixels, according to the third embodiment.

[0116] In Fig. 19, each amplifier 12 is arranged in the center of four pixels, and four photoelectric conversion elements 11 (e.g., q_{11}, q_{12}, q_{21}, q_{22}) are arranged as they surround the amplifier 12.

[0117] Further, a light-shield unit 17 is provided for each pixel in an area which is symmetry to a portion of the amplifier 12 occupying the pixel with respect to the center of the pixel. Therefore, the center of mass of each photoelectric conversion element 11 is in the center of each pixel. Accordingly, the centers of mass of the photoelectric conversion elements 11 (q_{11}, q_{12}, q_{21}, q_{22}, q_{31}, q_{32}, q_{41}, q_{42}) are arranged at a same interval, D, both in the row and column directions.

[0118] Fig. 20 shows another layout of amplifiers 12 in pixels when each amplifier 12 is arranged at the boundary of four pixels arranged in a 2 × 2 array in the row direction, and the four photoelectric conversion elements 11 (e.g., q_{11}, q_{12}, q_{21}, q_{22}) are arranged so as to sandwich each amplifier 12.

[0119] In addition, light-shield unit 17 is arranged in three peripheral areas, other than the peripheral area where the amplifier 12 occupies, of the pixel, as shown in Fig. 20. Therefore, the centers of mass of the photoelectric conversion elements 11 (q_{11}, q_{12}, q_{21}, q_{22}, q_{31}, q_{32}, q_{41}, q_{42}) are located at the same interval, D, both in the row and column directions.

[0120] The arrangement as shown in Fig. 20 is rotated by 90 degrees, namely, an arrangement in which row direction and column direction are exchanged, is also possible.

[0121] Further, in an arrangement as shown in Fig. 21, G filter, which contributes most to resolution, is arranged in the upper left pixel and the lower right pixel among four pixels configuring a unit cell 30. In the pixel covered by green filter (G pixel), a light-shield unit 17 is provided in an area which is symmetry to a portion of the amplifier 12, arranged at a central portion of the unit cell 30, occupying the pixel with respect to the center of the pixel. Therefore, the center of mass of the photoelectric conversion element 11 of the G pixel is at the center of the G pixel. With this configuration, intervals, D, of the photoelectric conversion elements q11 and q12 of G pixels become the same both in the row and column directions.

[0122] Further, a pixel covered by red filter (R pixel) is arranged in the upper right pixel in the unit cell 30, and a pixel covered by blue filter (B pixel) is arranged in the lower left pixel in the unit cell 30. These pixels do not have light-shield units, differing from the G pixels; however, since a single R pixel and a single B pixel are arranged in each unit cell 30, the intervals between adjacent R and B pixels become identical, namely 2D.

[0123] Fig. 22 is another layout of amplifiers 12 in pixels. In this layout, areas occupied by the amplifier 12 and the light-shield units 17 are reduced in the G pixels.

[Layout 1]

[0124] Fig. 23 shows a practical pattern layout of four photodiodes and an amplifier in the CMOS sensor 22 in Fig. 1.

[0125] The CMOS sensor, as shown in Fig. 23, is formed on a singlecrystalline silicon substrate based on a layout rule 0.4μm. Each pixel is a square, 8μm each side, and a source follower amplifier, as the amplifier 12, is shared by four pixels arranged in a 2 × 2 array. Therefore, the size of a unit cell 481, shown by a dash line, is 16μm × 16μm. A plurality of unit cells 481 are arranged in two dimensions.

[0126] Photodiodes 482a, 482b, 482c, and 482d are formed diagonally in each pixel, and the shapes of the photodiodes 482a to 482d are nearly symmetry with respect to the center of the unit cell 481 as well as symmetry with respect to vertical and horizontal lines passing over the center of the unit cell 481. Further, the center of mass (CM) of each photodiode is designed to be at the same position in each pixel. Further, reference numeral 495 denotes a light-shield unit.

[0127] Reference numeral 488a is a scanning line for controlling a transfer gate 483a; 490, a row selection line; and 492, a reset line for controlling a gate 493 of a MOS transistor.

[0128] Photo-charges accumulated in the photodiodes 482a to 482d are transferred to a floating diffusion (FD) portion 485 via transfer gates 483a to 483d, respectively. The size of the transfer gates 483a to 483d is L = 0.4μm, W = 1.0μm (L is a channel length and W is a channel width).

[0129] The FD portion 485 is connected to the gate 486 of a source follower via an aluminum (A1) wire having a width of 0.4μm, and the photo-charge transferred to the FD portion 485 modulates the gate voltage of the gate 486. The size of the MOS transistor of the gate 486 is L = 0.8μm, W = 1.0μm, and the total capacitance of the FD portion 485 and the gate 486 is about 5fF. Since Q = CV, the gate voltage of the gate 486 changes by 3.2 volts in response to the transference of 10^5 electrons.

[0130] Current flowing in from a V_{DD} terminal 491 is modulated by the MOS transistor of the gate 486, and transferred to a vertical signal line 487. Current flowing through the vertical signal line 487 is processed by a signal processing circuit (not shown) and formed into image information.

[0131] Thereafter, in order to set the potentials of the photodiodes 482a to 482d, the FD portion 485, and the gate 486 to the predetermined potential V_{DD}, the gate 486 of the MOS transistor connected to the reset line 482 is opened (at this time, the transfer gates 483a to 483d are also opened), thereby the photodiodes 482a to 482d, the FD portion 485, and the gate 486 are electrically connected to the V_{DD} terminal 491.

[0132] Thereafter, the transfer gates 483a to 483d are closed, thereby the accumulation of photo-charges in the photodiodes 482a to 482d start again.

[0133] In layout 1, the lines 488a to 488d, 490 and 492, passing over the unit cell 481 in the horizontal direction, are all formed with indium tin oxide, transparent conductor, of 1500Å thickness. Therefore, areas of the photodiodes 482a to 482d under the aforesaid lines can also receive light, and the center of mass of each photodiode matches the center of mass of light-receiving area of the photodiode.

[0134] According to the Layout 1 in the third embodiment, it is possible to provide a CMOS sensor with -relatively high area ratio and high aperture ratio, in which photodiodes are arranged at an equal pitch.

[Layout 2]

[0135] Fig. 24 shows another practical pattern layout of four photodiodes and an amplifier in the CMOS sensor 22.

[0136] Referring to Fig. 24, reference numerals 502a to 502b denote the photodiodes; 503a to 503d, transfer gates; 505, an FD portion; 506, the gate of a source follower; 507, a vertical signal line; 508a to 508d, scanning lines; 510, a row selection line; and 512, a reset line for controlling the gate 513 of a MOS transistor.

[0137] In layout 2 of the third embodiment, since three lines out of lines 508a to 508d, 510, and 512 pass through the central portion of each pixel. Therefore, if these lines are metal wires which shield light incoming toward the photodiodes 502a to 502d, the center of mass of the light-receiving area of each photodiode does not shift, and remains at the center of each pixel.

[0138] In layout 2 of the third embodiment, opaque metal wires with small resistance are generally used, time constant of the lines in the horizontal direction is improved, and a high-speed image sensing apparatus is obtained.

[0139] In the aforesaid layout 1 and layout 2 of the third embodiment, the portion under the shield unit is not effectively used. It is possible to extend the area of a photodiode, as a photoelectric conversion element, under the light-shield unit, and make the extended area function as a charge accumulation unit.

[Layout 3]

[0140] In layout 2 of the third embodiment, since the lines pass through the center of each pixel where light-receiving efficiency is high, sensitivity of the image sensing apparatus may not be good. Accordingly, an improved layout is shown in Fig. 26 as the layout 3 of the third embodiment. Fig. 26 is a practical pattern layout of the layout shown in Fig. 20.

[0141] In layout 3 of the third embodiment, transfer gates 523a to 523d, the gate 526 of a source follower, and the gate 533 of a MOS transistor for resetting are formed under scanning lines 528a to 528d, a row selection line 530, and a reset line 532; therefore, it is possible to maximize the size and aperture of each of photodiodes 522a to 522d. In addition, the aperture of each photodiode is at the center of each pixel. Further, light-shield units are formed in an area where horizontal and vertical wires are formed.

[0142] Further, in layout 3 of the third embodiment, the source follower, as the amplifier 12 shown in Fig. 20, and the MOS transistor for resetting are separately arranged in periphery of each photodiode in the row direction, thus, compactly arranged under wires running in the row direction.

[0143] Further, since there is a large area which is not yet used under wires in the upper right pixel, it is possible to add a new configuration, such as a smart sensor.

[0144] According to the layout 3 of the third embodiment, the area and aperture of a photodiode are increased comparing to the layout 2, it is possible to provide a high-sensitive image sensing apparatus with wide dynamic range. In addition, if the size of each pixel is further reduced and the size of the aperture of the photodiode becomes small, e.g., wavelength of light, each side, the problem such that light will not enter the photodiode will not arise. Thus, the layout 3 would remain

as an efficient layout for the future.

[0145] In layout 3 of the third embodiment, the amplifier 12 is arranged at the central portion of each unit cell, and the center of mass of a light-receiving area is designed to match the center of mass of a pixel. However, the present invention is not limited to this, and the shape of apertures of pixels may be arbitrarily designed as long as the shape is identical and arranged in a fixed position in every pixel, as shown in Fig. 27, for instance.

[0146] In other words, by designing the apertures to have the same shape and arranged in a predetermined position in each pixel, intervals between the centers of mass of light receiving areas become the same.

[Layout 4]

[0147] Fig. 28 shows a practical pattern layout, corresponding to Fig. 21, of four photodiodes and an amplifier in the CMOS sensor 22 in Fig. 1.

[0148] In layout 4 of the third embodiment, colors of a color filter and positions of the colors are predetermined. Specifically, in the four pixels arranged in a 2 × 2 array, the upper left and lower right pixels are covered with green filter (G pixels) which contributes most to luminance signals, the upper right pixel is covered with red filter (R pixel), and the lower left pixel is covered with blue filter (B pixel).

[0149] In layout 4, the amplifier 12 and other peripheral circuits are arranged so that photodiodes 542a and 542d of the G pixels have the maximum area and aperture ratio.

[0150] Further, the center of mass of light-receiving area of a G pixel matches the center of mass of the G pixel, thus, the intervals between the centers of mass of G pixels are equal.

[0151] According to the layout 4 of the third embodiment, it is possible to provide a high sensitive image sensing apparatus.

[On-chip Lens and Other Variations]

[0152] Fig. 29 shows an example when on-chip lens is used in the CMOS sensor 22 in Fig. 1.

[0153] Referring to Fig. 29, an on-chip lens 602 is formed on each pixel in a unit cell 601. Light incoming from outside of the CMOS sensor 22 is collected by the on-chip lens 602 and incidents on the aperture 603. Reference numeral 604 denotes an imaging area where light is gathered by the on-chip lens 602.

[0154] By controlling the design and the position of the on-chip lens, the position of the imaging area can be set relatively freely.

[0155] Thus, when a plurality of pixels share a single amplifier, if photodiodes, as photoelectric conversion elements, could not be arranged at a same interval, image signals as if they are obtained by photodiodes which are arranged at a same interval can be obtained by controlling the designs and positions of on-chip lenses.

[0156] Further, if an image sensing lens used in the image sensing apparatus is not telecentric, an incoming angle of light which incidents on a sensor chip in the central portion is different from an outer portion. Thus, by setting apertures of photodiodes in the outer portion of the CMOS sensor at different intervals, image signals as if they are obtained by photodiodes which are arranged at a same interval can be obtained.

[0157] According to the layout 1 to layout 4 of the third embodiment, light-shield units which are optical members are adjusted to make intervals between light-receiving areas identical. With the on-chip lens, the intervals of light receiving areas are made identical virtually by adjusting the designs and positions of the on-chip lenses, i.e., other optical members.

[0158] It should be noted that a configuration using an optical member, such as an on-chip lens, is also applicable to the first and second embodiments.

[Noise Reduction]

[0159] The inventors of the present application also have developed a signal read circuit for reducing noise suitably used in an image sensing apparatus having a configuration, as described above, in which a plurality of pixels share an amplifier.

[0160] Fig. 30 is a circuit diagram of a unit cell of the CMOS sensor having any of the aforesaid configurations.

[0161] Referring to Fig. 30, references q_{11}, q_{12}, q_{21}, and q_{22} are photodiodes as photoelectric conversion elements; M_{TX1} to M_{TX4}, MOS transistors for transferring photo-charges accumulated in the photodiodes q_{11}, q_{12}, q_{21}, and q_{22} to a floating diffusion (FD) portion; M_{RES}, a MOS transistor for resetting the FD portion; and M_{SF} and M_{SEL}, MOS transistors configuring a source follower. The MOS transistor M_{SEL} also functions as a selection switch for selecting a photodiode.

[0162] Next, an operation of the image sensing apparatus including a signal processing circuit according to the third embodiment is explained. Fig. 31 is an equivalent circuit of the image sensing apparatus including the signal processing unit.

[0163] Fig. 32 is a timing chart for operating the image sensing apparatus shown in Fig. 31.

[0164] Referring to Figs. 31 and 32, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal ϕTX_{R0} which is applied to a reset line 573 of the first row is activated during a horizontal blanking period (i.e., when a signal ϕHBL is high), and signals for subsequent lines are applied in the same manner. Accordingly, all the pixels in every row are reset to the reset potential V_{DD}.

[0165] In each horizontal blanking period, as shown in Fig. 32, during a period T_{11}, a signal ϕL becomes high and a transistor 561, connected for a vertical signal line 557, is turned on and the vertical signal line 557 is reset.

Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors 562-1 to 562-3 are turned on. Accordingly wires in the upstream of transistors for reading signal, 564-1 to 564-3, and capacitors 563-1 to 563-3 (C_{TN}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line 557, and reset. Accordingly, residual charges in the capacitors 563-1 to 563-3, for instance, are removed.

[0166] Thereafter, in a period T_{12}, a signal ϕTX_{RO} to be applied to the reset line 573 is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors M_{SF} and M_{SEL} in each unit cell, is reset to the voltage V_{DD}.

[0167] Then, in a period T_{13}, a signal ϕRV becomes high and a transistor 560 for grounding, connected to the vertical signal line 557, is turned on, and the vertical signal line 557 is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor 563-1 (C_{TN}) for storing a noise component to the vertical signal line 557, and the transistor 562-1 is turned on. At this time, a signal ϕS_O to be applied to a row selection line 574 is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor M_{SF} flows from a V_{DD} terminal to the capacitor 563-1 (C_{TN}), thereby the capacitor 563-1 (C_{TN}) stores charge corresponding to the noise component.

[0168] Next, in a period T_{14}, a signal ϕTX_{OOO} applied to the odd-column scanning line 571 is changed to high, in turn, a transfer gate (MOS transistor M_{TX1}, in this case) for an odd-number column in an odd-number row is turned on, and photo-charge accumulated in the photodiode q_{11} is transferred to the floating gate of the MOS transistor M_{SF}. The capacitor 563-1 (C_{TN}) for storing the noise component is disconnected from the vertical signal line 557 when the signal ϕT_N becomes low, and the capacitor 563-2 (C_{TS1}) for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the photodiode q_{11}, for instance, in an odd-number column in an odd-number row is stored in the capacitor 563-2 (C_{TS1}) via the vertical signal line 557.

[0169] Next, in a period T_{15}, the signal ϕL becomes high, and only the vertical signal line 557 is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1}, and ϕT_{S2}, are low, other portions are not reset, and their states are preserved.

[0170] Next, the signal ϕTX_{RO} applied to the reset line 573 is changed to high between periods T_{15} and T_{16}, and the gate of the source follower amplifier (i.e., the gate of MOS transistor M_{SF}) is reset to the potential V_{DD}.

[0171] In the period T_{16}, a signal ϕTX_{OeO} applied to a scanning line 572 is changed to high, and photo-charge accumulated in the photodiode q_{12} in an even-number column in an odd-number row is transferred to the floating gate of the MOS transistor M_{SF}. At this time, the signal ϕT_{S2} is changed to high, and photo-charge accumulated in the photodiode p_{12} is stored in the capacitor 563-3 (C_{TS2}) via the vertical signal line 557, in the similar manner.

[0172] In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors 563-1, 563-2, and 563-3 (C_{TN}, C_{TS1}, C_{TS2}) by each column for a row.

[0173] Next, in a period T_{17}, in order to sequentially transfer the charges stored in the capacitors 563-1 to 563-3 (C_{TN}, C_{TS1}, C_{TS2}) to amplifiers 566-1 to 566-3, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register 559, and transistors 564-1 to 564-3, provided for each column, are turned on; thereby the capacitors 563-1 to 563-3 (C_{TN}, C_{TS1}, C_{TS2}) are connected to the respective amplifiers 566-1 to 566-3. From the capacitors 563-1 to 563-3 (C_{TN}, C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier 567-1, a signal S1 obtained by subtracting the noise component from the first signal is outputted, and a signal S2 obtained by subtracting the noise component from the second signal is outputted from a differential amplifier 567-2. Note that accumulation of photo-charges by the photodiodes are also performed during the period T_{17}.

[0174] Further, by changing signals ϕTX_{OOe} and ϕTX_{Oee} to high instead of the signals ϕTX_{OOO} and ϕTX_{OeO} in the aforesaid operation, signals corresponding to photo-charges accumulated in the photodiodes q_{21} and q_{22} in an even-number row are read out and a noise component is subtracted from those photo-charge signals to obtain the signals S1 and S2.

<First Modification of the Third Embodiment>

[0175] Next, another configuration of an image sensing apparatus including a signal processing circuit is explained.

[0176] Fig. 33 is an equivalent circuit of the image sensing apparatus including the signal processing unit.

[0177] In the modification 1, four capacitors 563-2 to 563-5 (C_{TS1} to C_{TS4}) are provided for storing photo-charge signals, and different information can be stored in the respective capacitors 563-2 to 563-5. More specifically, a signal corresponding to photo-charge accumulated in the photodiode q_{11} is stored in the capacitor 563-2 (C_{TS1}), and a signal corresponding to photo-charge accumulated in the photodiode q_{22} is stored in the capacitor 563-5 (C_{TS4}), for instance. Therefore, processes performed in the downstream of amplifiers 566 may be operated at a half clock speed to achieve the same throughput of the image sensing apparatus having the configuration shown in Fig. 31. Accordingly, the amplifiers 566, the differential amplifiers 567, and other signal processing circuits may be also operated at a half clock speed comparing to the configuration shown in Fig. 31. Thus, required speed of the operating elements is decreased, and it is possible to use inexpensive lower performance elements to configure the circuit. As a result, the cost of the system is reduced.

[0178] Note, the charges to be stored in the capacitors are not limited to those respectively corresponding to photo-charges accumulated in the respective photodiodes, and added charges may be stored by controlling operation of the transfer gates and the reset MOS. When the CMOS sensor 22 has the configuration as shown in Fig. 21, for instance, it is possible to store a photo-charge signal of the G photodiode q_{11} in the capacitor 563-2 (C_{TS1}), a photo-charge signal of the G photodiode q_{22} in the capacitor 563-3 (C_{TS2}), and a photo-charge signal of the R photodiode q_{12} and the B photodiode q_{21} in the capacitor 563-4 (C_{TS3}). It is effective to apply this configuration to a smart sensor using each pixel more intelligently.

[0179] According to the configuration as explained in the third embodiment and the first modification of the third embodiment, it is possible to reduce noise caused by variation in characteristics of amplifiers each provided for each unit cell.

<Second Modification of the Third Embodiment>

[0180] Next, a case of operating the image sensing apparatus of the second modification of the third embodiment will be explained with reference to Figs. 34 and 35. Fig. 34 is an equivalent circuit of an image sensing apparatus including a signal processing circuit, and Fig. 35 is a timing chart for operating the image sensing apparatus shown in Fig. 34.

[0181] First, during a horizontal blanking period, photo-charges accumulated in pixels are transferred and photodiodes are reset to an initial state.

[0182] During a period T_{21}, the vertical signal lines 557 are reset by changing a signal ϕR_V to high to remove residual charges on the vertical signal lines 557. At the same time, residual charges in the capacitors C_{TN1}, C_{TN2}, C_{TS1}, C_{TS2} are removed by changing signals ϕT_{N1}, ϕT_{N2}, ϕT_{S1}, and ϕT_{S2} to high.

[0183] During a period T_{22}, in advance of transferring photo-charges of photodiodes in odd-number columns in a first row (q_{11}, q_{13}, ..., $q_{1(n-1)}$), the gates of amplifiers (the gates of the MOS amplifiers M_{SF}) are reset by changing a signal ϕTX_{RO} to high and residual charges in the gates are removed. After resetting the gates, reset noise remains.

[0184] During a period T_{23}, the reset noise from the period T_{22} and offset voltages of the amplifiers are transferred to capacitors C_{TN1}. The output terminals of the amplifiers are electrically connected to the vertical signal lines 557 by changing a signal ϕS_O to high, and a signal ϕL is also changed to high to turn on MOS transistors 561 for activating the amplifiers. Further, a signal T_{N1} is changed to high to electrically connect the capacitors C_{TN1} with the respective vertical signal lines 557. Accordingly, noise is stored in the capacitors C_{TN1}.

[0185] During a period T_{24}, photo-charges of photodiodes in odd-number columns in a first row (q_{11}, q_{13}, ..., $q_{1(n-1)}$) are transferred to the capacitors C_{TS1}. By changing the signals ϕL, ϕT_{S1}, and ϕS_O to high, the amplifiers and the capacitors C_{TS1} are electrically connected.

[0186] When a signal ϕTX_{OO} becomes high, photo-charge is transferred from each photodiode in the odd-number column in the first row to the amplifier. With this operation, the photo-charge is added to the reset noise from the period T_{22} at the gate of the amplifier. This gate voltage is further superposed on the offset voltage, and a signal (S1 + N1) is stored in each capacitor C_{TS1}.

[0187] During the periods T_{25} to T_{28}, photo-charges of photodiodes in even-number columns in the first row (q_{12}, q_{14}, ..., q_{1n}) are transferred to the capacitors C_{TS2}. The basic operation is the same as that performed during the periods T_{21} to T_{24}, except a signal ϕTX_{Oe} is changed to high instead of the signal ϕTX_{OO}, a signal ϕT_{N2} is changed to high instead of the signal ϕT_{N1}, and a signal ϕT_{S2} is changed to high instead of the signal ϕT_{S1}.

[0188] During a period T_{29}, residual charges in the vertical signal lines 557, the amplifiers, and the transfer MOS are removed, thereby transference of reset noise and photo-charge signals are completed.

[0189] After the aforesaid processes, noise signals N1 and N2, and signals (S1 + N1) and (S2 + N2) are stored in the capacitors C_{TN1}, C_{TN2}, C_{TS1}, and C_{TS2}, respectively. These signals are outputted via horizontal signal lines in response to signals $\phi H1$ and $\phi H2$ controlled by a horizontal shift register 559 during a period T_{210}. Then, in a differential amplifier A1, the noise signal N1 is subtracted from the signal (S1 + N1), thereby a signal S1 is outputted, and in a differential amplifier A2, the noise signal N2 is subtracted from the photo-charge signal (S2 + N2), thereby a signal S2 is outputted.

[0190] Accordingly, photo-charge signals faithfully corresponding to the photo-charges accumulated in the photodiodes q_{11} to q_{1n} in the first row are obtained. Charging operation starts when photo-charges are transferred to the gate in the period T_{24} and T_{28}.

[0191] In the next horizontal blanking period, -the same operation performed for the first row as described above is repeated for the second row. After reading out the photo-charges of photodiodes in the second row, the amplifier, shared by four pixels, are put into a disconnected state until the next vertical blanking period when next operation is performed.

[0192] In order to read out photo-charges by two rows, another set of capacitors C_{TN1}, C_{TS1} and C_{TS2}, and differential amplifiers A1 and A2 are to be added to the configuration shown in Fig. 34. More specifically, in the aforesaid operation, photo-charges are read out by a single row in a non-interlace operation, whereas photo-charges of two rows are read out in one horizontal period.

[0193] Fig. 36 is a timing chart during a vertical blanking period.

[0194] While a single vertical blanking period, the aforesaid operation performed during the horizontal blanking period is repeated number-of-row times. The

vertical shift register outputs operation pulses ϕTX_{OO}, ϕTX_{Oe}, ϕTX_{RO}, and ϕS_O for each horizontal blanking period for each row.

[0195] As described above, in the second modification of the third embodiment, in addition to removing noise due to variation in characteristics of amplifiers as described in the third embodiment and in the first modification of the third embodiment, reset noise is also removed.

<Fourth Embodiment>

[0196] Next, the fourth embodiment of the present invention will be explained.

[0197] In the fourth embodiment, a case where an additional function is added to an amplifier, a common circuit in the aforesaid embodiments, shared in a unit cell is explained.

[0198] Fig. 37 shows a configuration of the common circuit with the additional function.

[0199] In the downstream of an amplifier 701, memory 702, a differential amplifier 703, and a comparator 704 are added. The noise, as described in the foregoing embodiments, is temporarily stored in the memory 702, a signal (S - N) is transferred to the positive terminal of the differential amplifier 703, and the differential amplifier 703 takes the difference between the noise and the signal (S - N), thereby, a signal S, including no noise component, is obtained. The signal is transferred to a vertical signal line. Or, depending upon utilization purpose of the signal, the obtained signal can be digitized by the comparator 704.

[0200] Further, by replacing the comparator 704 with an analog-digital (A/D) converter, a digital signal can be obtained. The digital signal output from the A/D converter may be either a serial signal or a parallel signal. The circuit may be arbitrary changed depending upon utilization purpose.

<Other Embodiments>

[0201] The present invention is not limited to a general CMOS sensor as shown in Figs. 41 or 42, and may be applied to an image sensor as disclosed in ISSCC98/SESS:ON11/IMAGESENSORS/PAPER FA11.8pp182, shown in Fig. 38.

[0202] In this case, a configuration of an amplifier shared by e.g., four photodiodes, may be the one as shown in Fig. 39.

[0203] Further, the present invention is not limited to a CMOS sensor, and applicable to any APS sensors.

[0204] Furthermore, in the first to fourth embodiments, a plurality of photoelectric conversion elements are arranged to share a single amplifier, forming a unit cell altogether, however, the amplifier may be replaced by other unit which processes signals, outputted from a plurality of photoelectric conversion elements. For instance, an A/D conversion circuit (USP No. 5,431,425) and a signal processing circuit, e.g., an image compressor (Journal of Television Society vol. 150, no. 3, pp.335 to 338, 1995) may be used in place of the amplifier.

[0205] The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore to apprise the public of the scope of the present invention, the following claims are made.

Claims

1. An image sensing apparatus having a plurality of unit cells (13-16), each including a plurality of photoelectric conversion elements (11) and a common circuit (12) shared by said plurality of photoelectric conversion elements, arranged in either one or two dimensions,
   wherein said plurality of photoelectric conversion elements are arranged at a predetermined interval.

2. The image sensing apparatus according to claim 1, wherein said plurality of photoelectric conversion elements (11) in each unit cell are arranged side by side in one direction, and said common circuit (12) is arranged at the edge of each plurality of photoelectric conversion elements.

3. The image sensing apparatus according to claim 1 or 2, wherein said plurality of photoelectric conversion elements (11) in each unit cell are arranged side by side in one direction, and said common circuit (12) is arranged between adjoining unit cells arranged in a direction perpendicular to the direction of the arrangement of said plurality of photoelectric conversion elements.

4. The image sensing apparatus according to claims 1 to 3, wherein said common circuit (12) is arranged at the edge of each plurality of photoelectric conversion elements (11) arranged in a horizontal direction.

5. The image sensing apparatus according to claim 4, wherein said unit cell (13, 14) is configured with a plurality of pixels each including a photoelectric conversion element (11), and a number of horizontal conductors (38, 39, 40, 42) passing over each pixel is the same.

6. The image sensing apparatus according to any of claims 1 to 3, wherein said common circuit (12) is arranged at the edge of each plurality of photoelectric conversion elements (11) arranged in a vertical direction.

7. The image sensing apparatus according to claim 6, wherein said unit cell (15, 16) is configured with a plurality of pixels each including a photoelectric conversion element (11), and a number of vertical conductors passing over each pixel is the same.

8. The image sensing apparatus according to claim 4 or 6, wherein said unit cell (13-16) is configured with a plurality of pixels each including a photoelectric conversion element (11), and contacts between layers of each pixel are arranged so that a number of conductors (31, 37) passing over each unit cell, as well as one of the contacts which is not connected to a conductor passing over the unit cell is connected to a light-shield film of the pixel.

9. An image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements (11) and a common circuit (12) shared by said plurality of photoelectric conversion elements, arranged in two dimensions,

wherein photoelectric conversion elements (p_{12}, p_{14}, p_{21}, p_{23}), out of said plurality of photoelectric conversion elements, which are covered by a color filter that contributes mostly to forming a luminance signal are arranged in a same interval both in the horizontal and vertical directions by arranging adjoining rows or columns of photoelectric conversion elements shifted from each other.

10. The image sensing apparatus according to claim 9, wherein the adjoining rows or columns of said photoelectric conversion elements (p_{12}, p_{14}, p_{21}, p_{23}), covered by the color filter that contributes mostly to forming a luminance signal, are shifted by 3/2 pitches from each other.

11. The image sensing apparatus according to claim 9 or 10, wherein said plurality of photoelectric conversion elements (11) in each unit are arranged on both sides of said common circuit (12).

12. The image sensing apparatus according claim 11, wherein a color filter covering one of said plurality of photoelectric conversion elements (11) arranged on one side of said common circuit (12) contributes to forming a luminance signal, and a color filter covering another photoelectric conversion element arranged on the other side of said common circuit contributes to forming a color signal.

13. The image sensing apparatus according to any of claims 9 to 12, further comprising signal processing means (87-1, 87-2) for forming a luminance signal and a color difference signal on the basis of signals obtained from said plurality of photoelectric conversion elements (11).

14. An image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements (11) and a common circuit (12) shared by said plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising:

adjustment means (17, 602) for adjusting centers of mass of light-receiving areas of said plurality of photoelectric conversion elements provided in a central portion of the image sensing apparatus, so as to be apart at a same spatial interval.

15. The image sensing apparatus according to claim 14, wherein said adjustment means (17, 602) is an optical member.

16. The image sensing apparatus according to claim 15, wherein said optical member (17) is a light-shield unit.

17. The image sensing apparatus according to claim 16, wherein said light-shield unit (17) is arranged between adjoining unit cells.

18. The image sensing apparatus according to claim 16, wherein a plurality of light-shield units (17) are arranged so as to be symmetry with respect to a horizontal or vertical line passing over a center of each unit cell (30).

19. The image sensing apparatus according to any of claims 14 to 16, wherein apertures of said plurality of photoelectric conversion elements (11) are placed at a fixed position in each pixel.

20. The image sensing apparatus according to claim 15, wherein said optical member (602) is an on-chip lens.

21. The image sensing apparatus according to any of claims 14 to 20, wherein apertures are adjusted so that centers of mass of light-receiving areas of said photoelectric conversion elements (11) in a peripheral area of the image sensing apparatus are at a same interval.

22. The image sensing apparatus according to any of claims 14 to 19, wherein centers of mass of light-receiving areas of said plurality of photoelectric conversion elements matches the respective centers of mass of pixels.

23. The image sensing apparatus according to any of claims 14 to 22, wherein each of said unit cells (481) has a conductor (188-a to 188-d, 490, 492) passing over the unit cell in a predetermined direction, and said conductor is a transparent conductor.

24. The image sensing apparatus according to any of claims 14 to 22, wherein each of said unit cells (501) has a conductor (508-a to 508-d, 510, 512) passing over the unit cell in a predetermined direction, and said conductor passes through centers of a plurality of pixels each including a photoelectric conversion element (11).

25. The image sensing apparatus according to any of claims 14 to 22, wherein each of said unit cells (521) has a conductor (528-1 to 528-d, 530, 532) passing over the unit cell in a predetermined direction, and said conductor is provided over one side portion of each of a plurality of pixels each including a photoelectric conversion element (11), and said photoelectric conversion element is arranged in the other portion of the pixel.

26. The image sensing apparatus according to any of claims 14 to 22, wherein each of said unit cells (521) includes conductors (527, 528-1 to 528-3, 530 to 532), and each of a plurality of pixels each including a photoelectric conversion element (11) has a same number of conductors on each side.

27. The image sensing apparatus according to claim 25 or 26, wherein said common circuit (12) is arranged under the conductor (527, 528-a to 528-d, 530 to 532).

28. The image sensing apparatus according to any of claims 14 to 27, wherein said common circuit (12) is arranged at a central portion of each unit cell (481, 501, 541).

29. An image sensing apparatus having a plurality of unit cells (541), each including a plurality of photoelectric conversion elements (11) and a common circuit (12) shared by said plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising:

adjustment means (17, 555) for adjusting centers of mass of light-receiving areas of photoelectric conversion elements (142a, 142d) selected from said plurality of photoelectric conversion elements, provided in a central portion of the image sensing apparatus, on the basis of a predetermined condition, so as to be apart at a same spatial interval.

30. The image sensing apparatus according to claim 29, wherein at least one (142a, 142d) of said photoelectric conversion elements in each unit cell (541) is selected under the predetermined condition.

31. The image sensing apparatus according to claim 29 or 30, wherein the predetermined condition is that a photoelectric conversion element is covered by a color filter which contributes mostly to forming a luminance signal.

32. The image sensing apparatus according to any of claims 29 to 31, wherein said adjusting means (17) is a light-shield unit.

33. The image sensing apparatus according to any of claims 1 to 32, further comprising:

noise reading means (82-1, 83-1, 162-1, 163-1, 562-1, 563-1) for reading a noise of said common circuit (12);
first signal reading means (82-2, 83-2, 162-2, 163-2, 562-2, 563-2) for reading a first signal through said common circuit;
second signal reading means (82-3, 83-3, 162-3, 163-3, 562-3, 563-3) for reading a second signal through said common circuit; and
noise reduction means (87-1, 87-2, 567-1, 567-2) for reducing the noise from said first and second signals.

34. The image sensing apparatus according to any of claims 1 to 32, further comprising:

noise reading means (562, 563-1) for reading a noise of said common circuit (12);
signal reading means (562, 563-2 to 563-5) for reading a plurality of signals through said common circuit; and
noise reduction means (567) for reducing the noise from said plurality of signals.

35. The image sensing apparatus according to claim 33 or 34, wherein said noise reduction means (87-1, 87-2, 567-1, 567-2, 567) is differential means.

36. The image sensing apparatus according to claim 33, wherein said first signal is read from one of said plurality of photoelectric conversion elements (11) in each unit cell, and said second signal is read from another photoelectric conversion element in the same unit cell.

37. The image sensing apparatus according to claim 33, wherein said first signal is read from one of said plurality of photoelectric conversion elements (11) in each unit cell, and said second signal is read from the photoelectric conversion element and another photoelectric conversion element in the same unit cell.

38. The image sensing apparatus according to claim 34, wherein said first signal is read from one of said plurality of photoelectric conversion elements (11) in each unit cell, and said second signal is read from

other plural photoelectric conversion elements in the same unit cell.

39. The image sensing apparatus according to any of claims 1 to 38, wherein said common circuit (12) is an amplifier for amplifying and outputting a signal from each of said plurality of photoelectric conversion element (11).

40. The image sensing apparatus according to claim 39, wherein said common circuit (12) further includes transfer means for transferring the signal from each of said plurality of photoelectric conversion element (11) and reset means for resetting said common circuit.

41. The image sensing apparatus according to any of claims 1 to 38, wherein said common circuit (12) is digital signal conversion means for converting a signal from each of said plurality of photoelectric conversion element (11) into a digital signal.

42. The image sensing apparatus according to any of claims 1 to 38, wherein said common circuit (12) is a signal processing unit.

43. An image sensing system having the image sensing apparatus (22) according to any of claims 1 to 42, a lens system (21) for forming an image on the image sensing apparatus, and a signal processing circuit (23) for processing an output signal from the image sensing apparatus.

FIG. 1

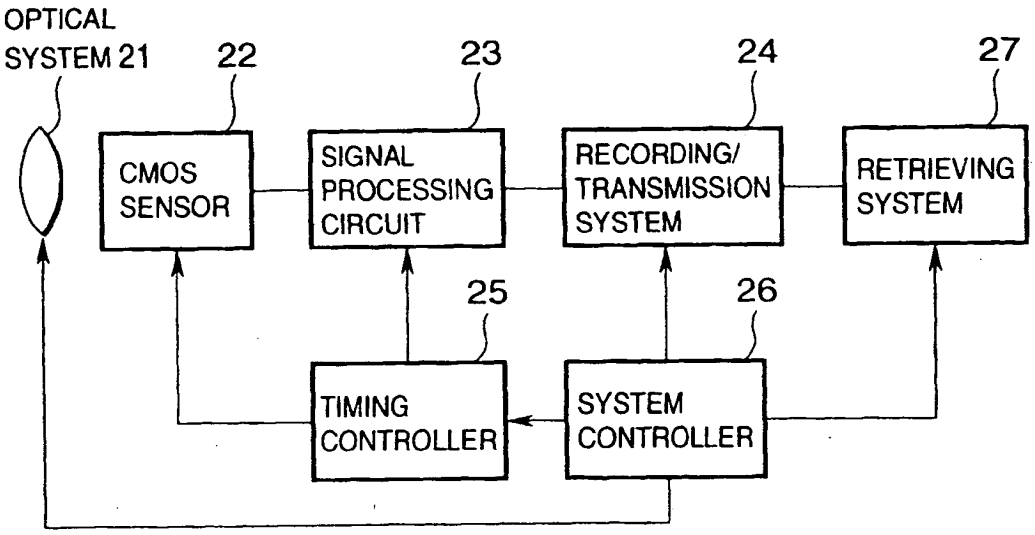


FIG. 2A

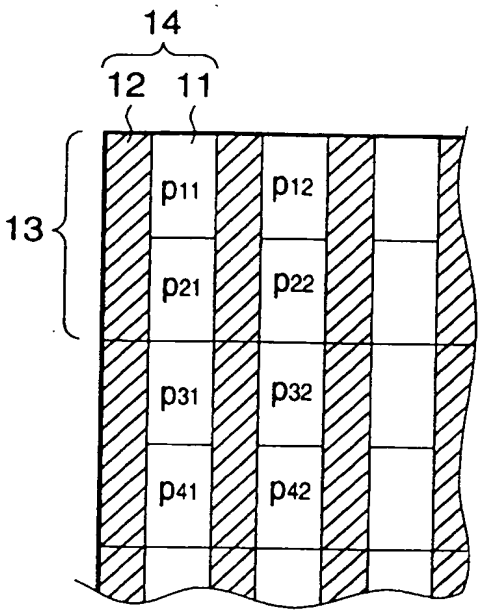


FIG. 2B

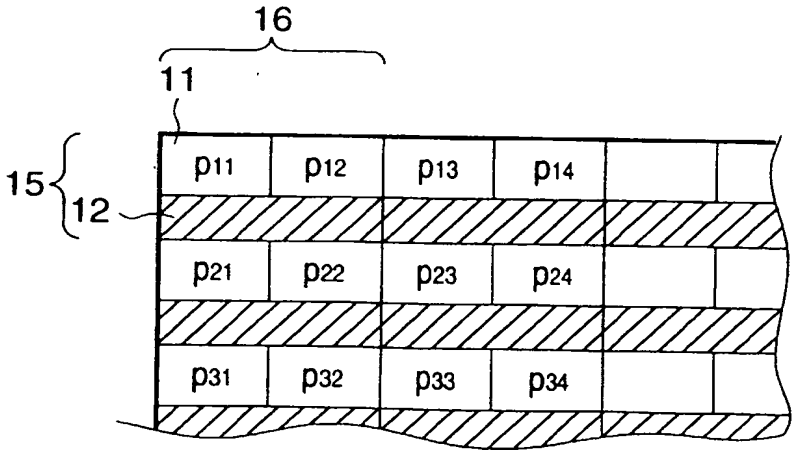


FIG. 3

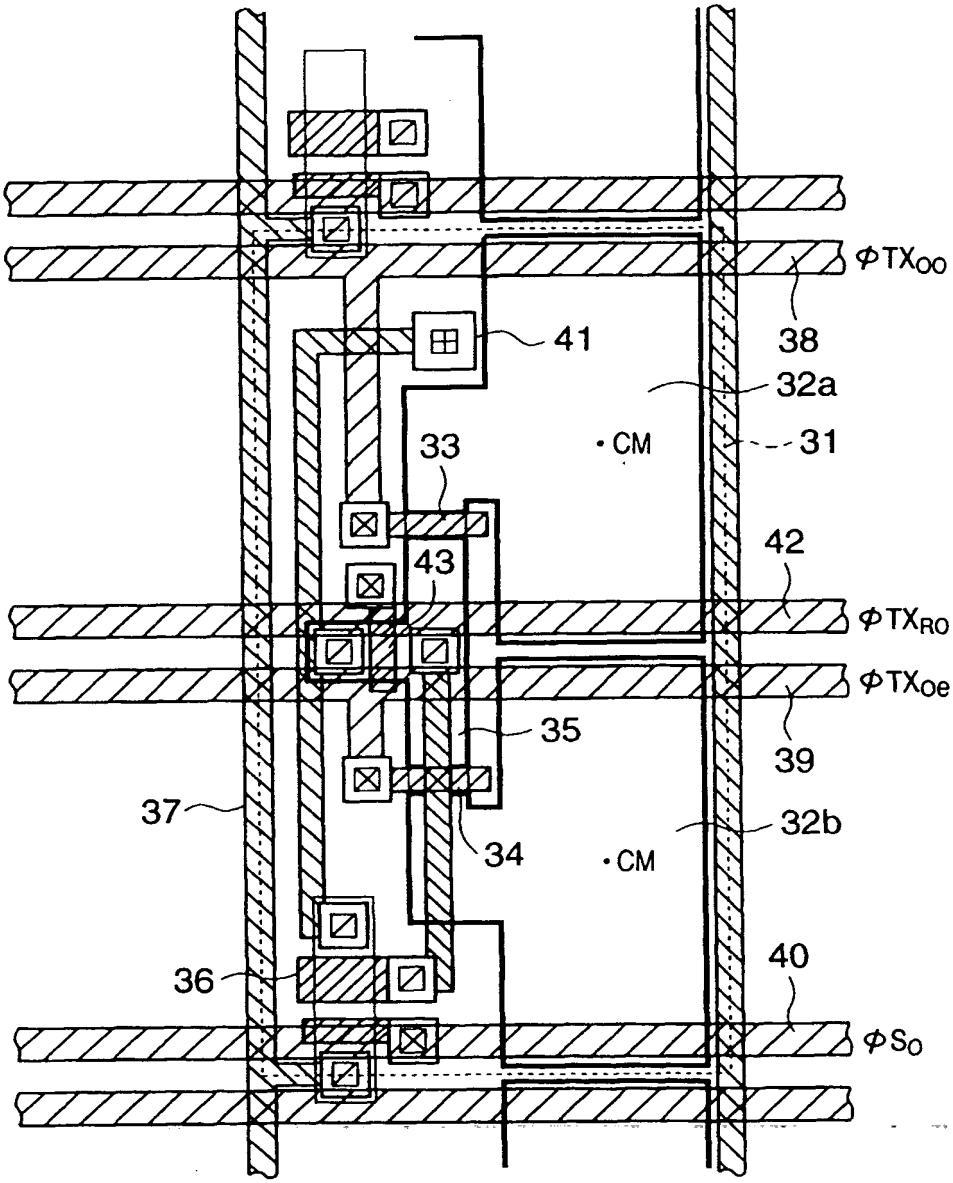


FIG. 4

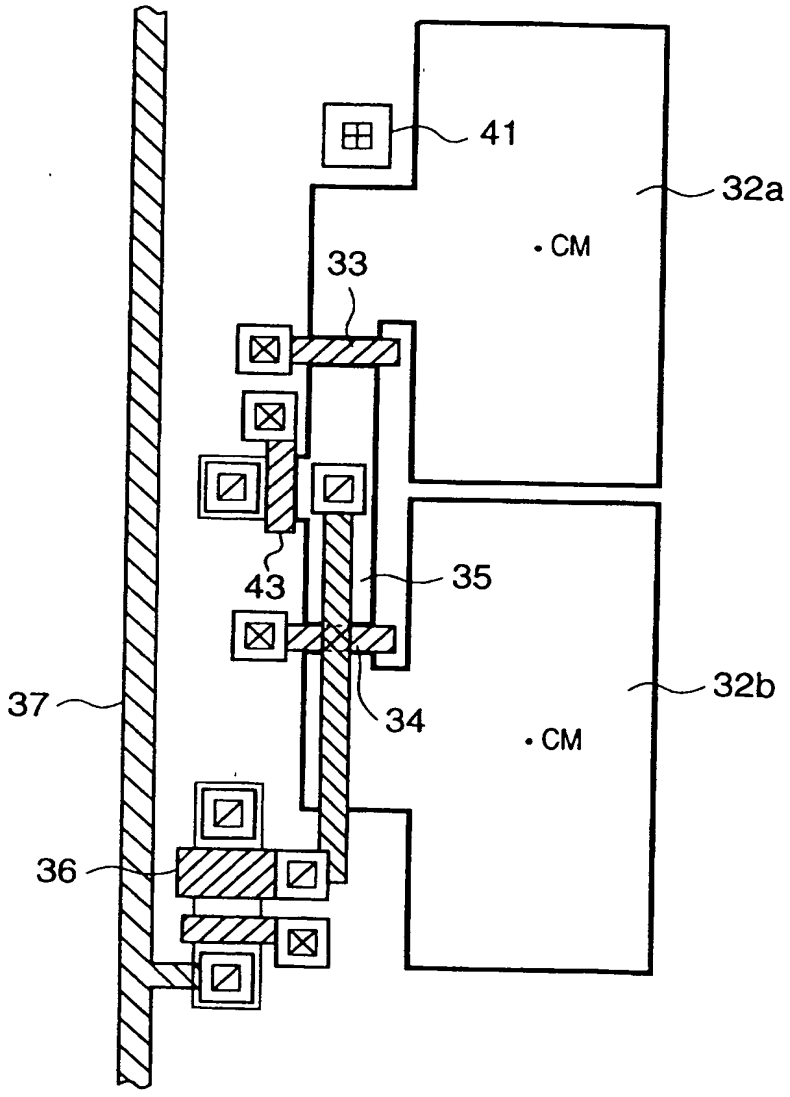


FIG. 5

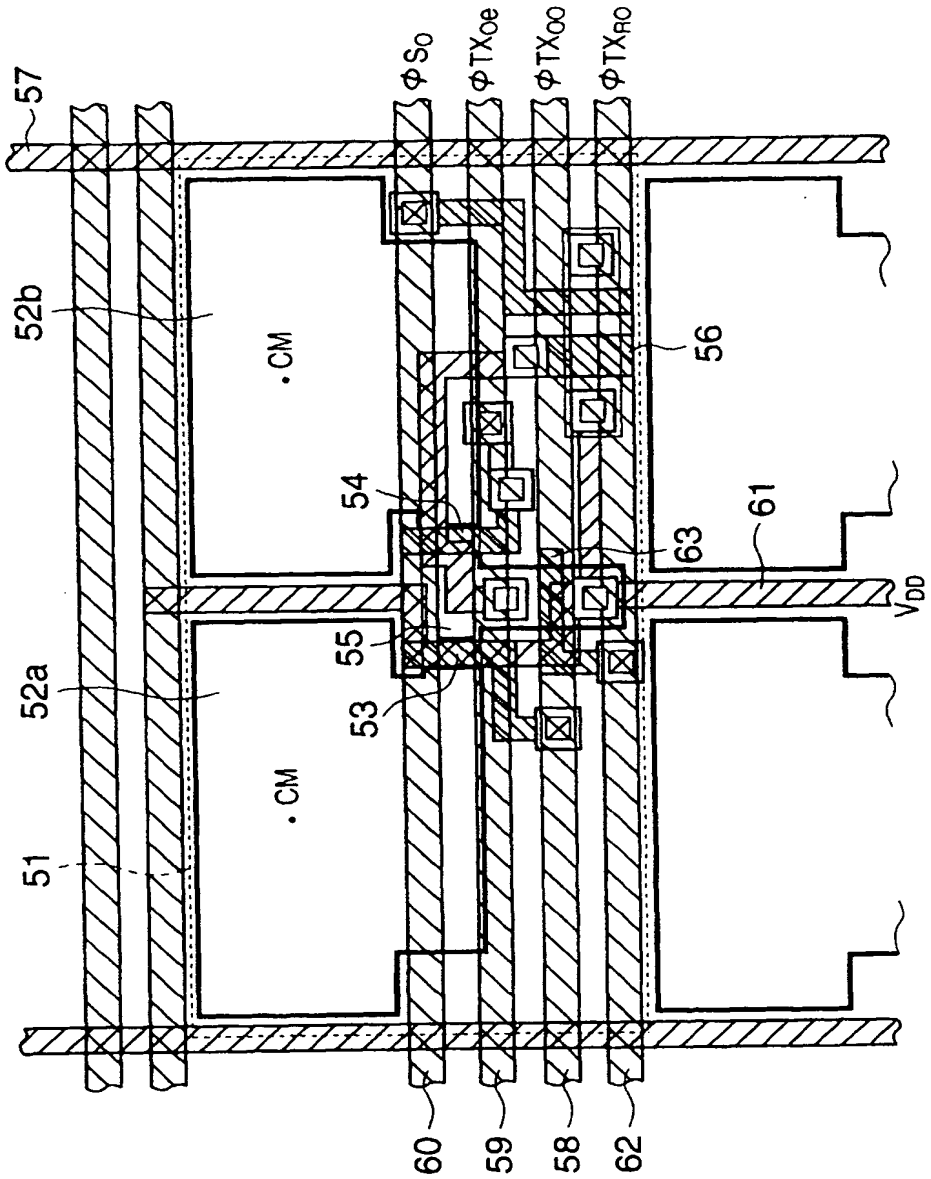


FIG. 6

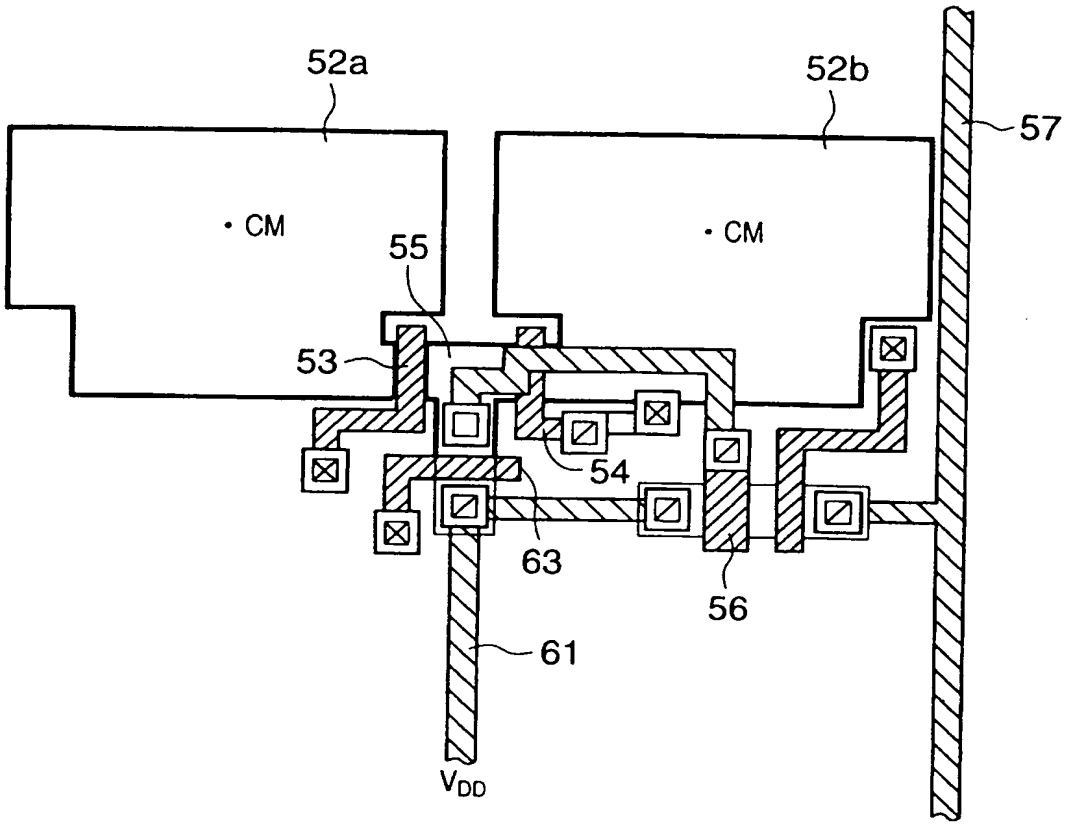


FIG. 7

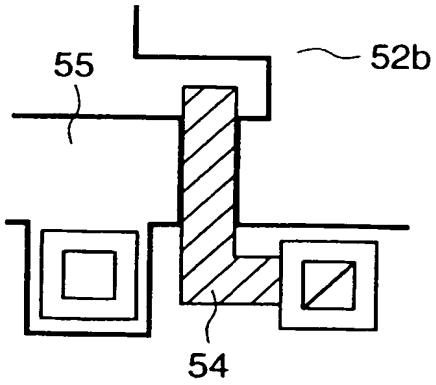


FIG. 8

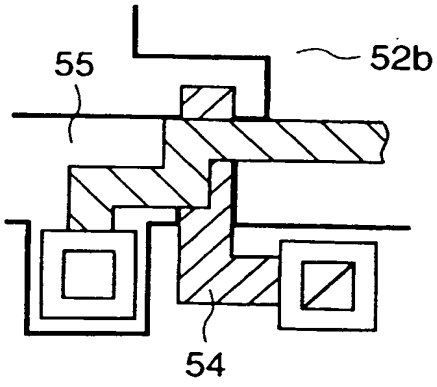


FIG. 9

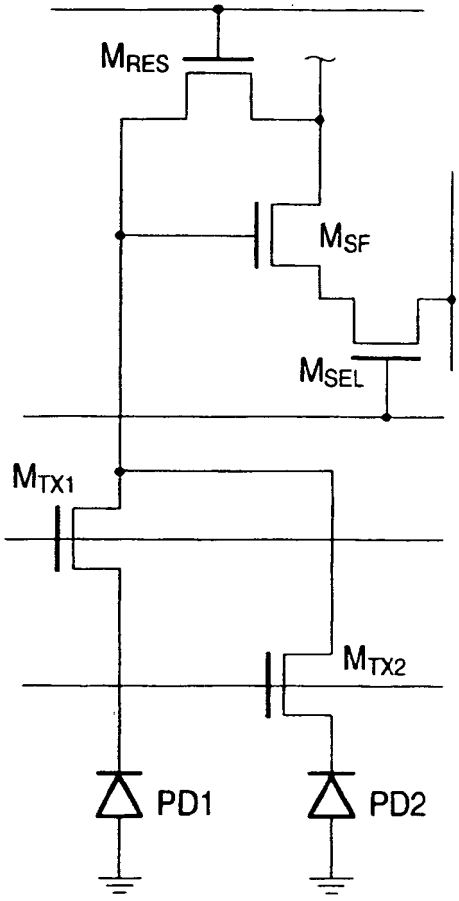


FIG. 10

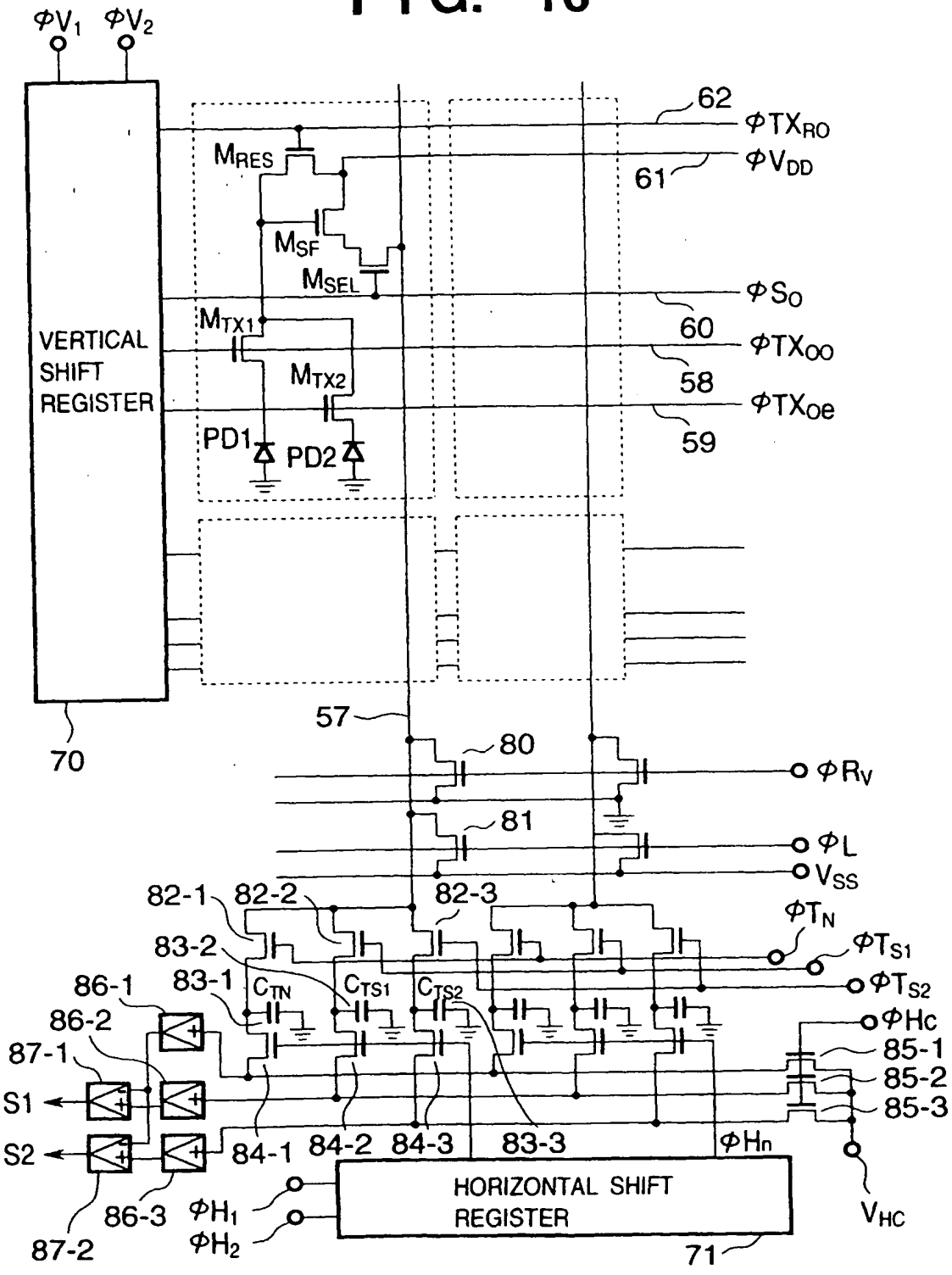


FIG. 11

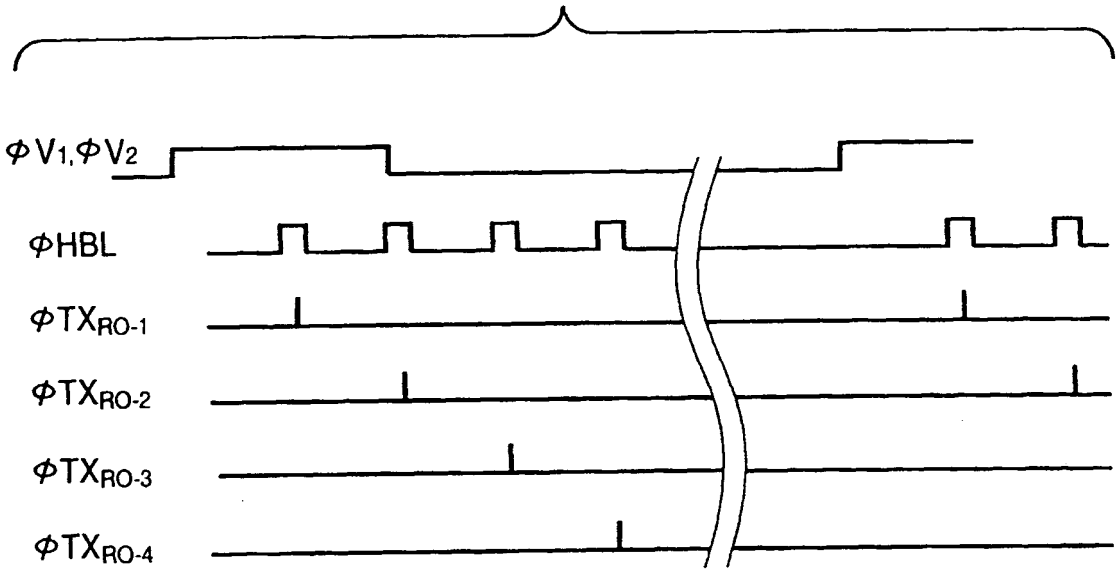


FIG. 12

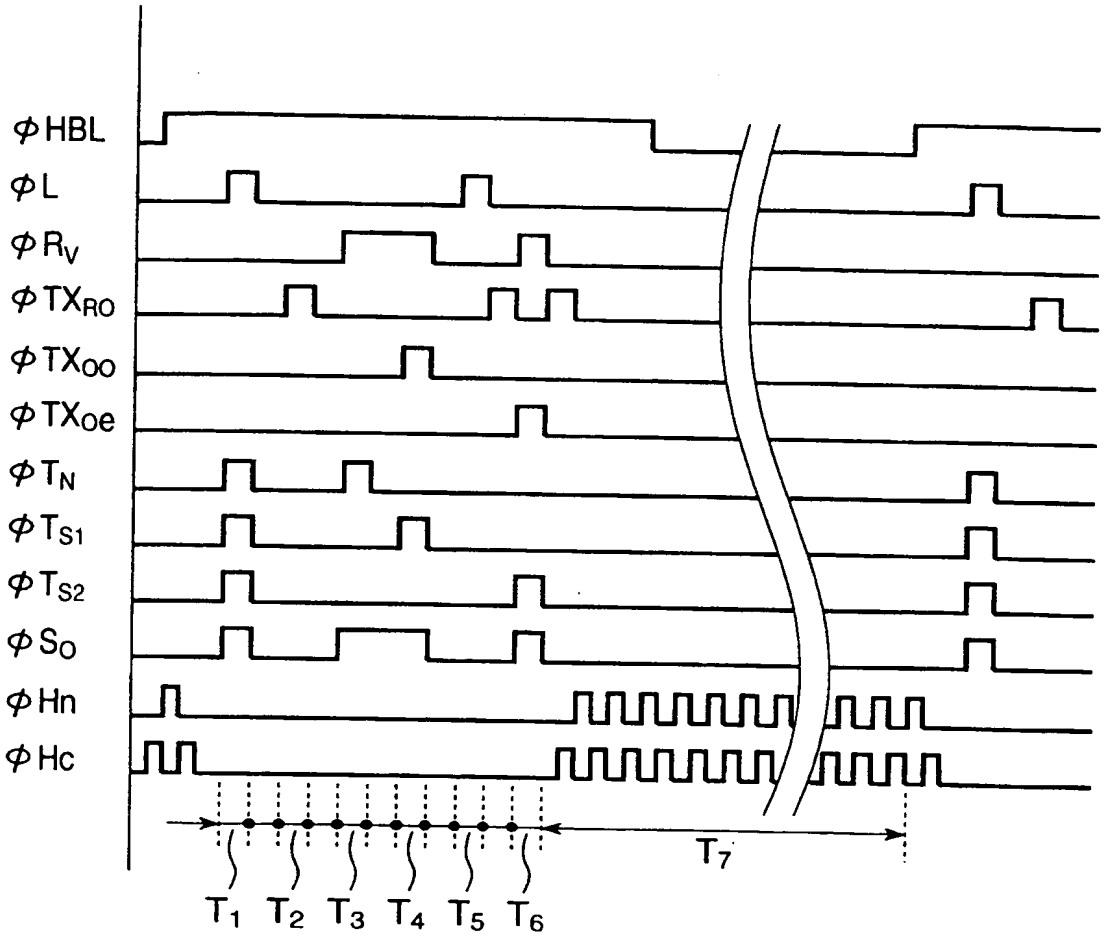


FIG. 13

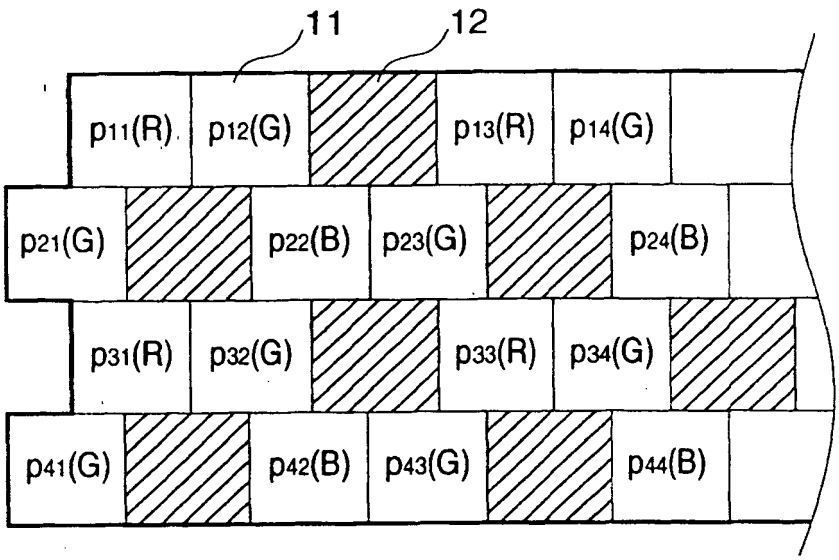


FIG. 14

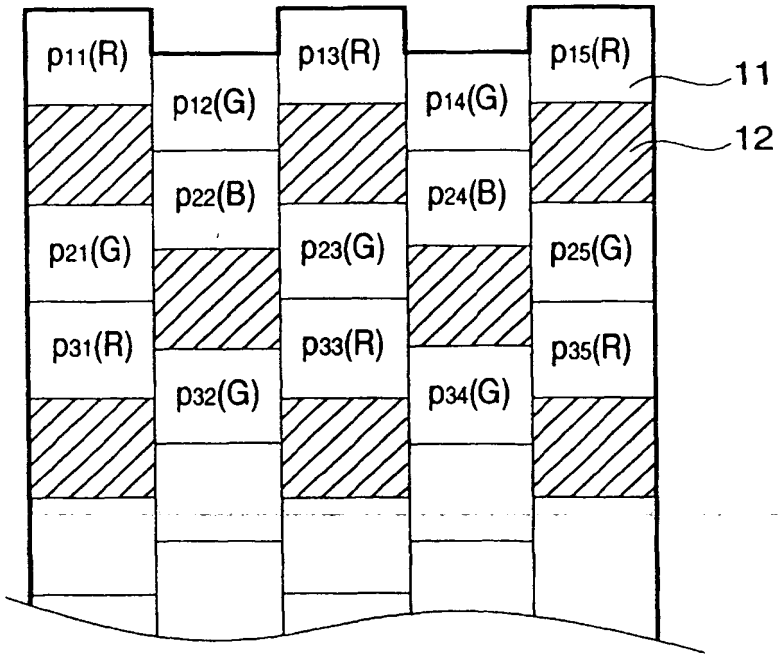


FIG. 15

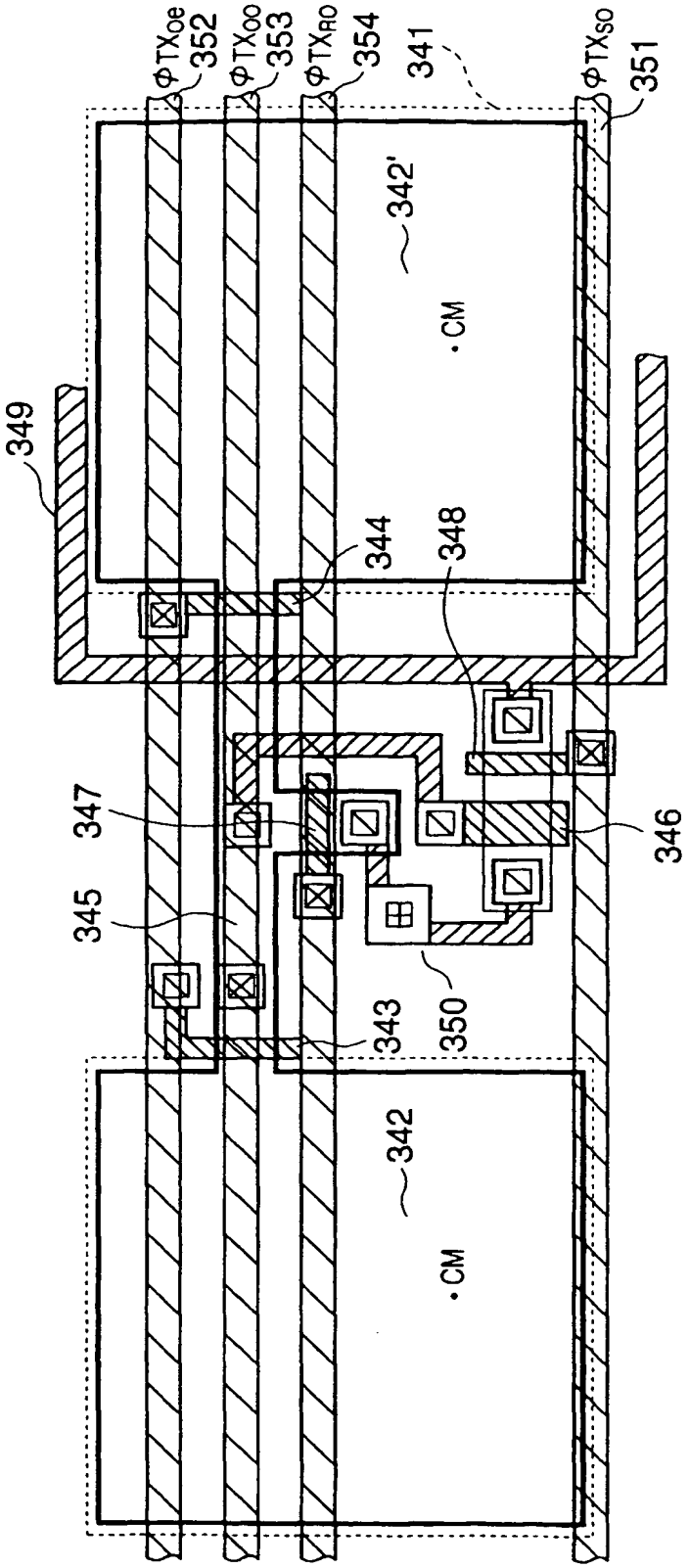


FIG. 16

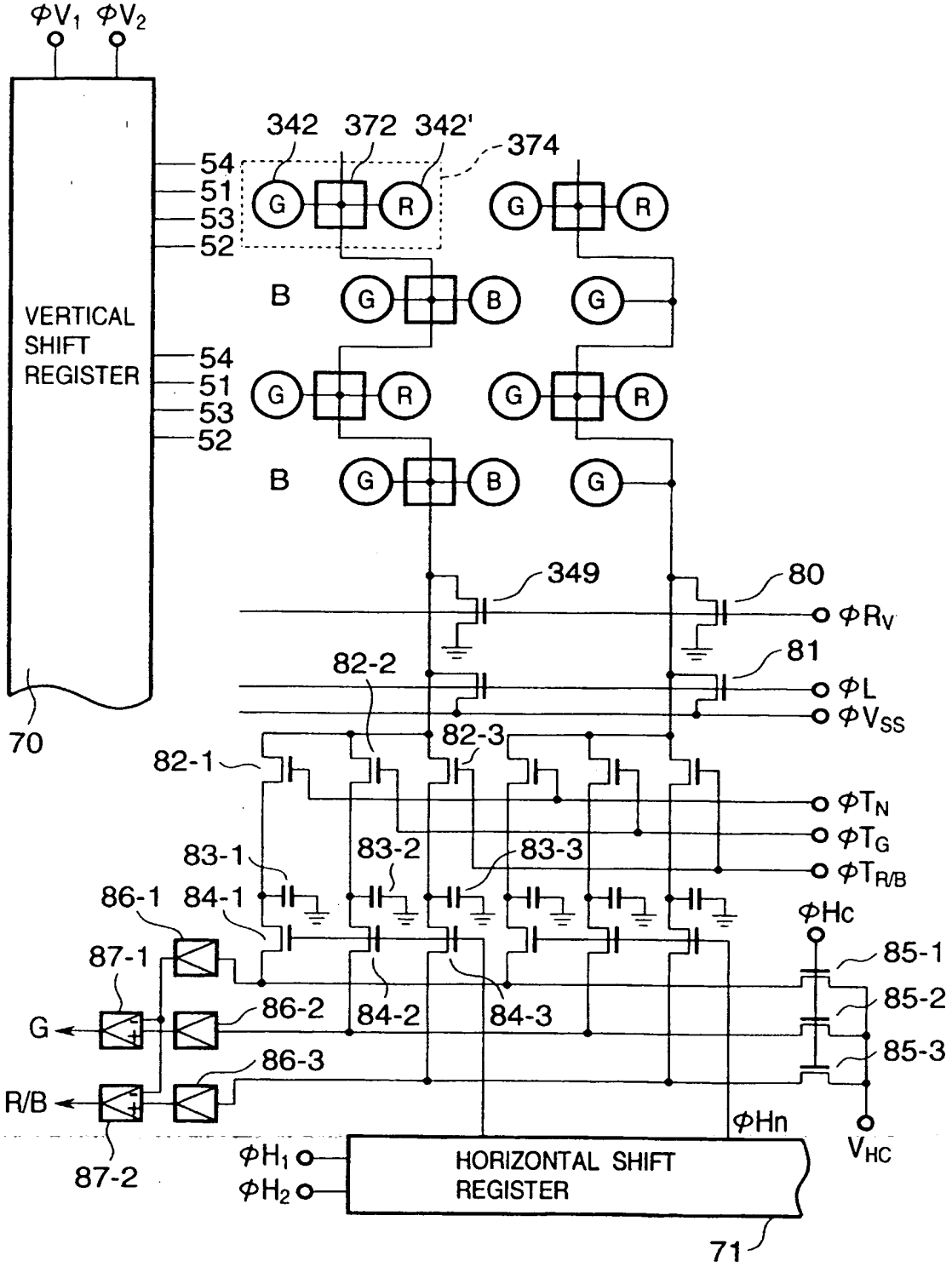


FIG. 17

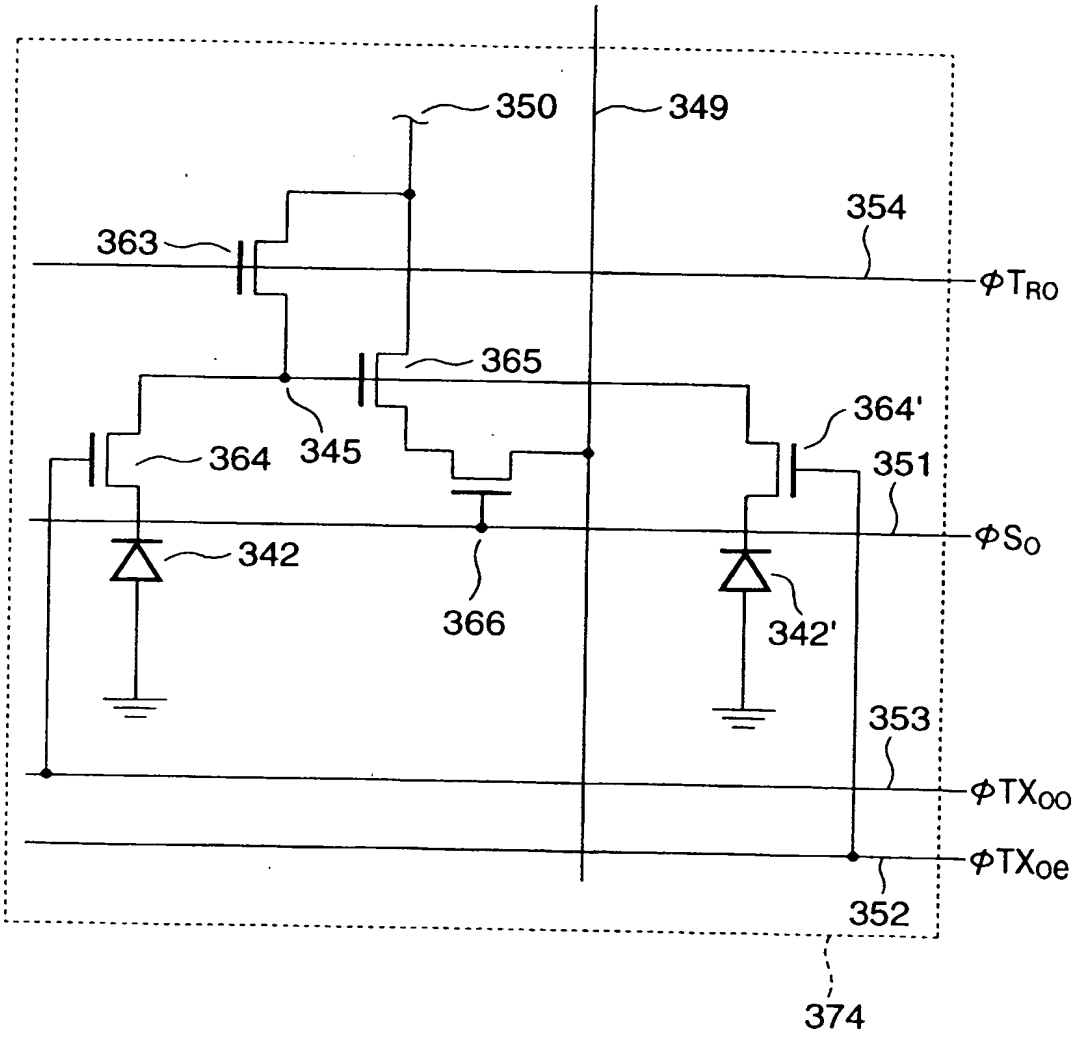


FIG. 18

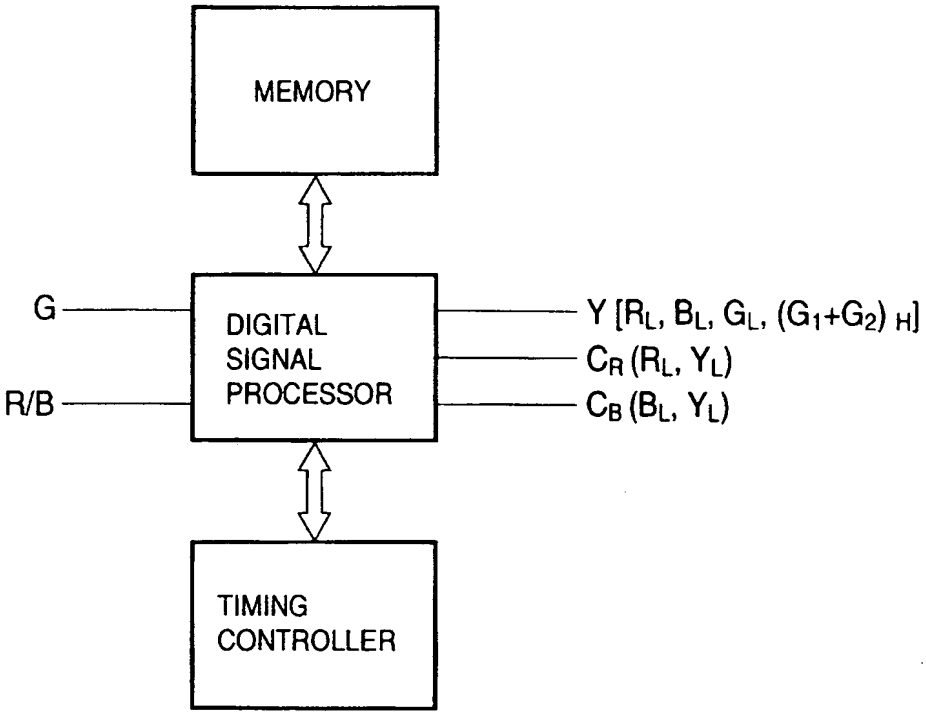


FIG. 19

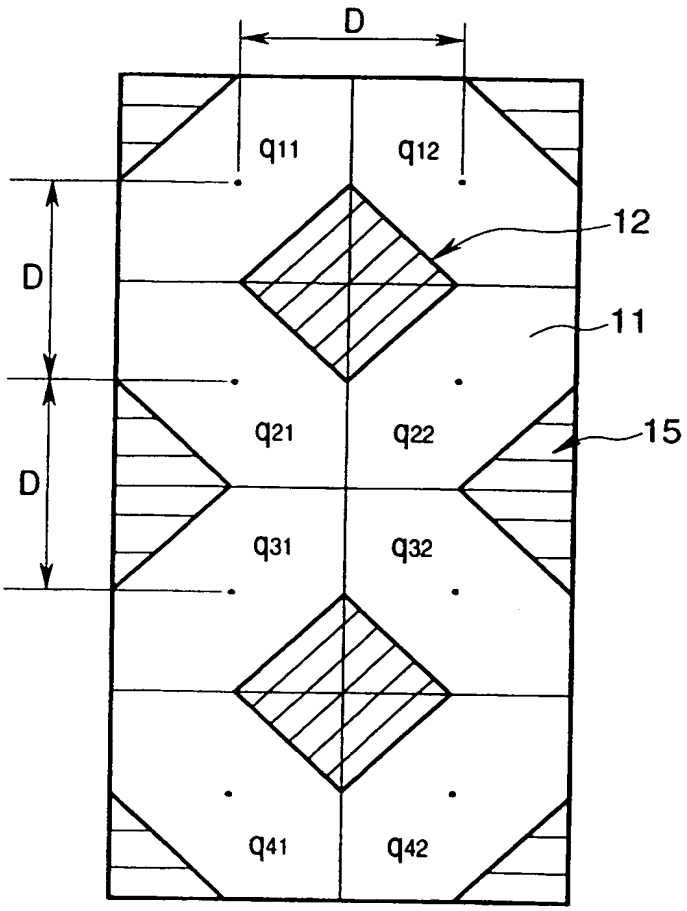


FIG. 20

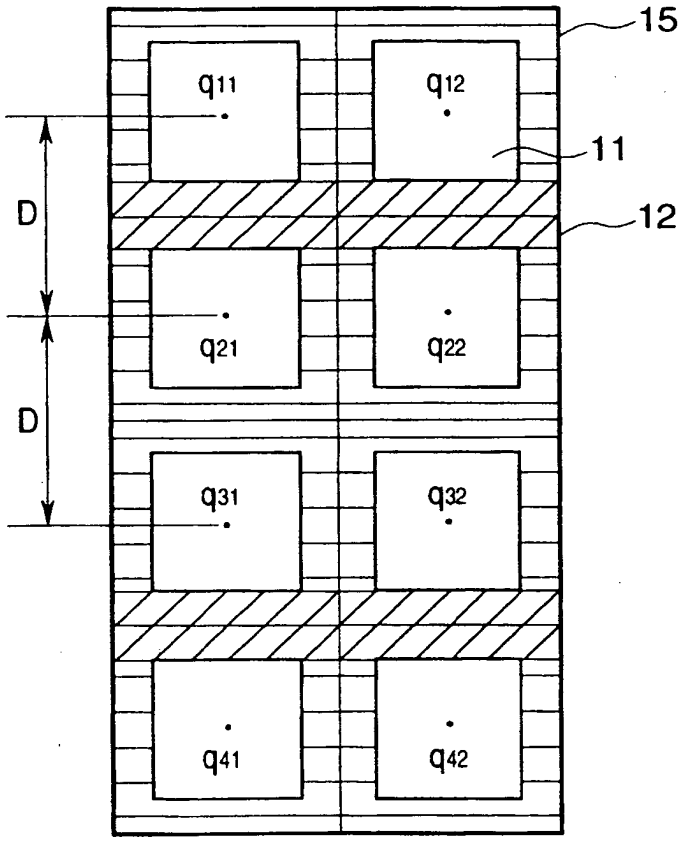


FIG. 21

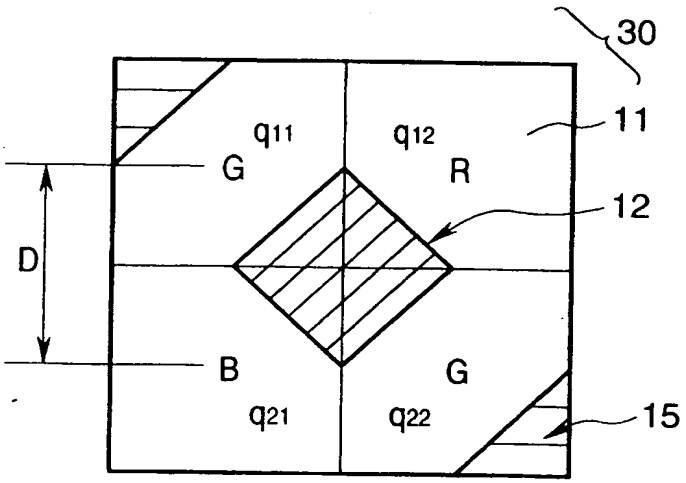


FIG. 22

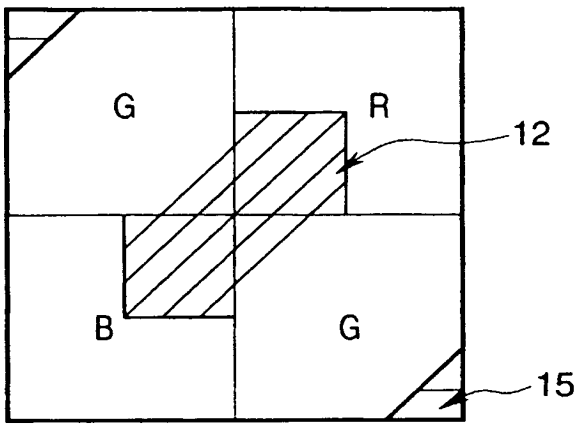


FIG. 23

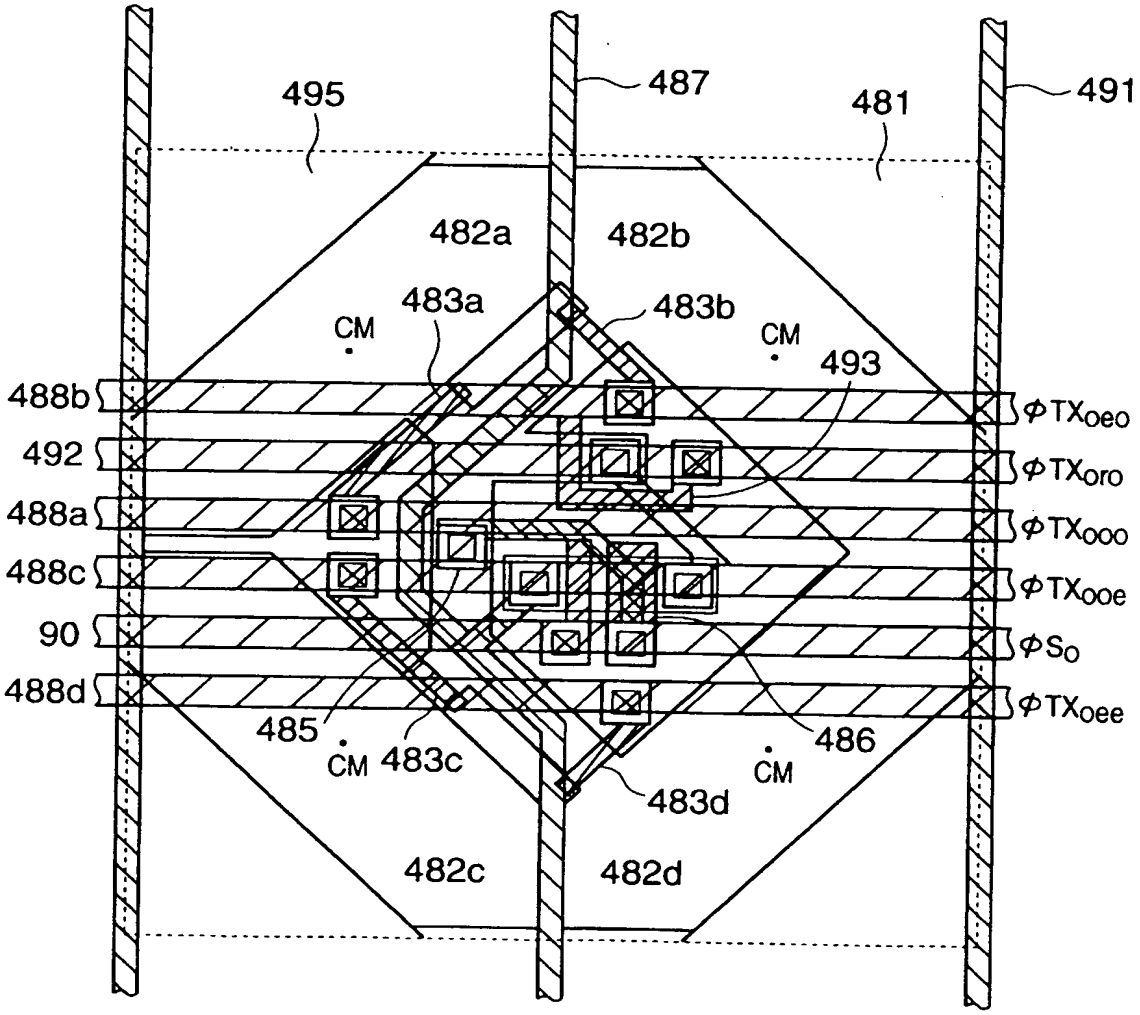


FIG. 24

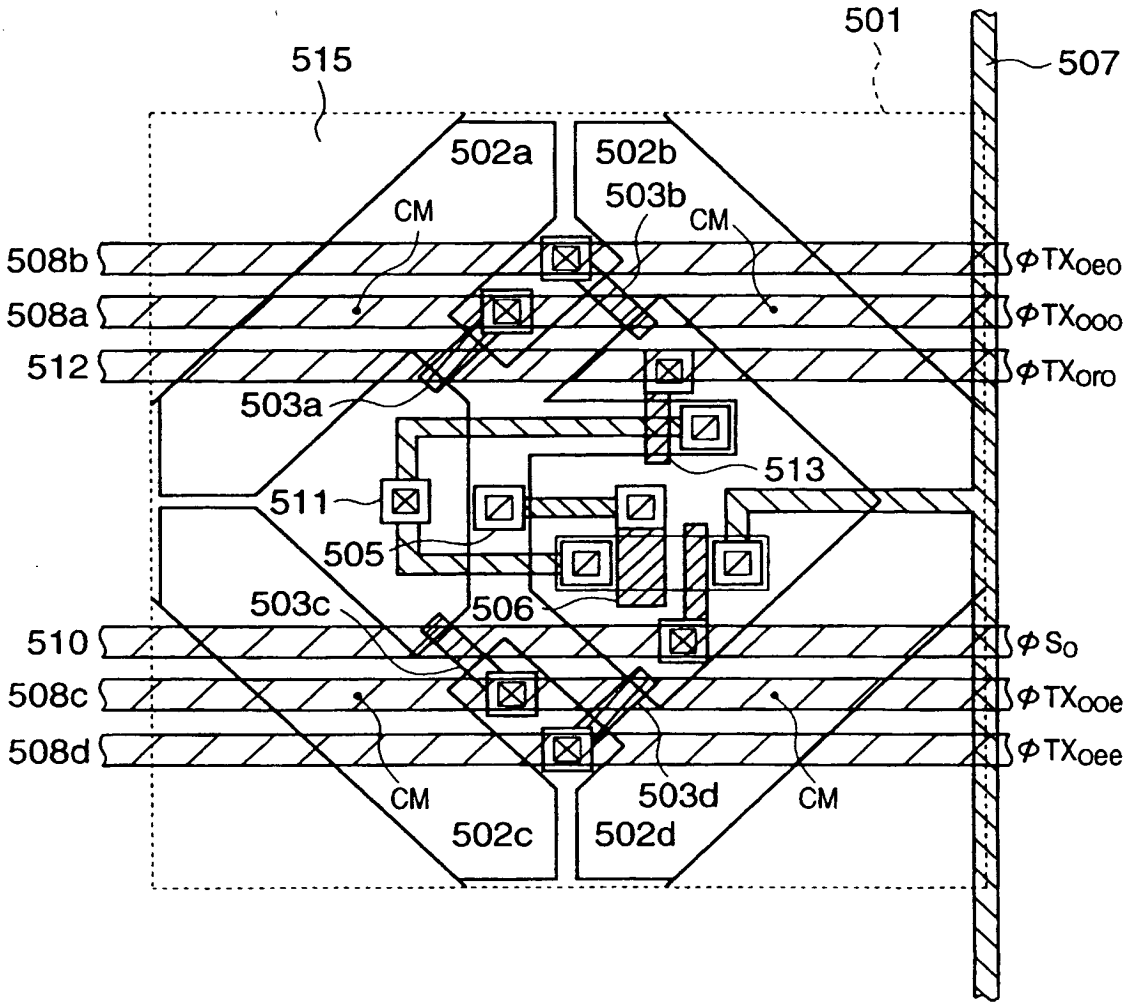


FIG. 25

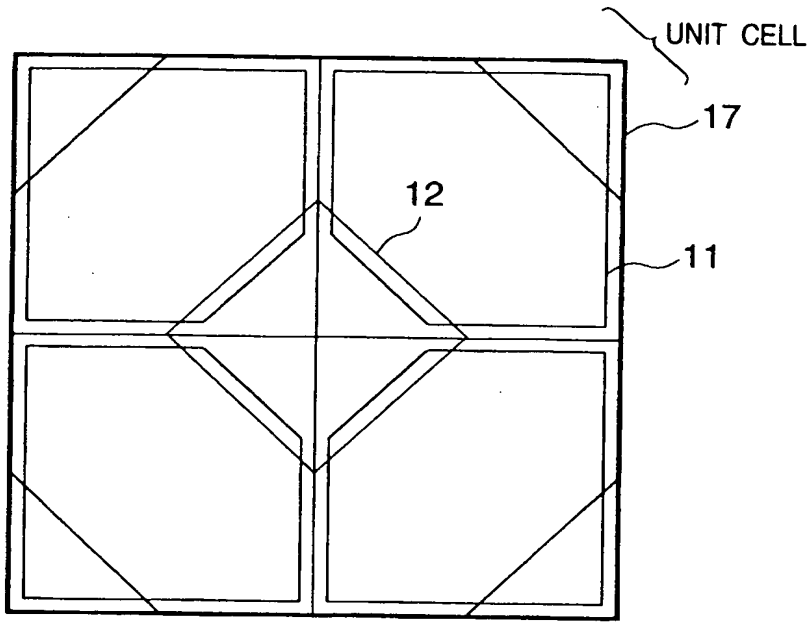


FIG. 26

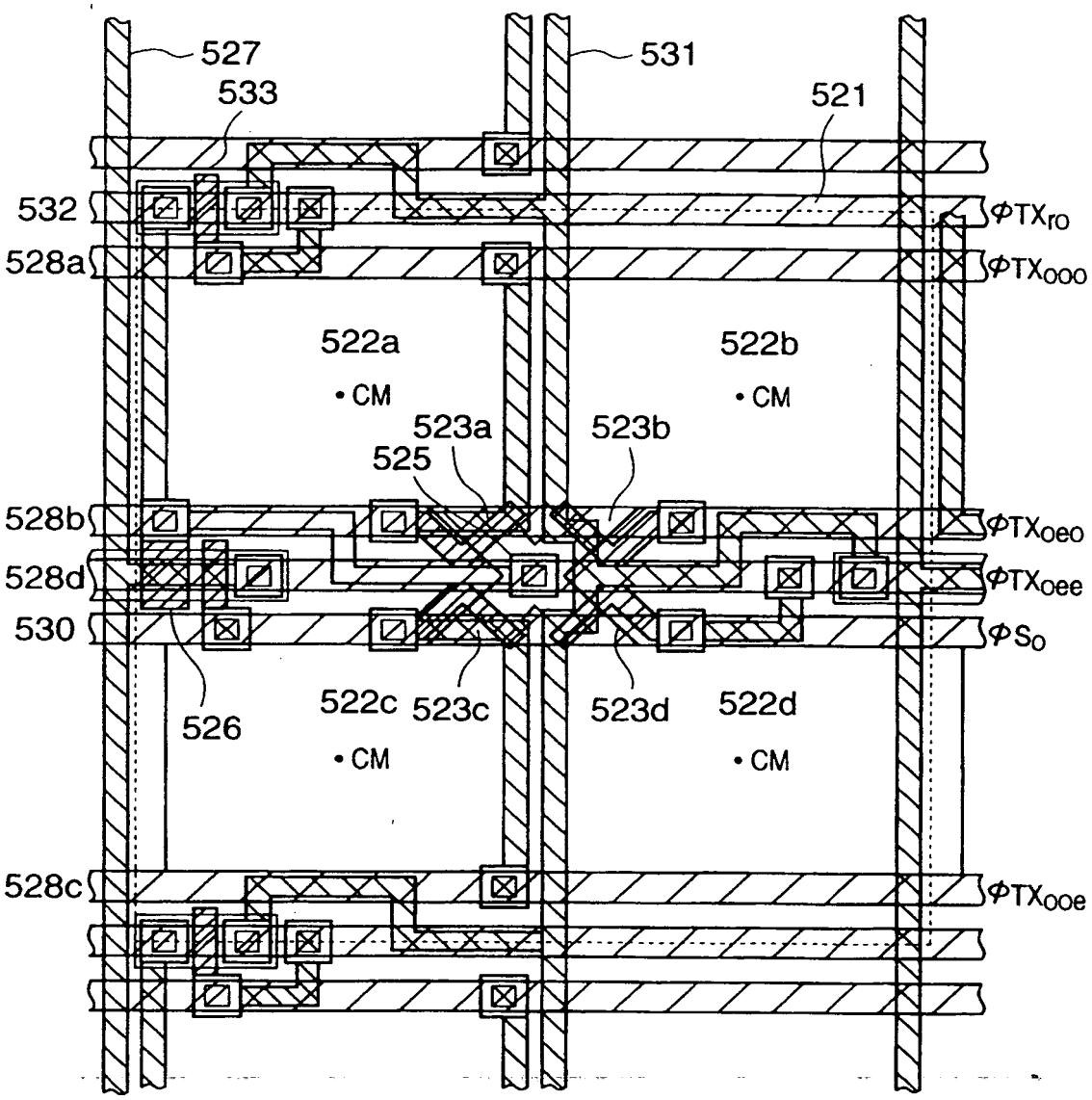


FIG. 27

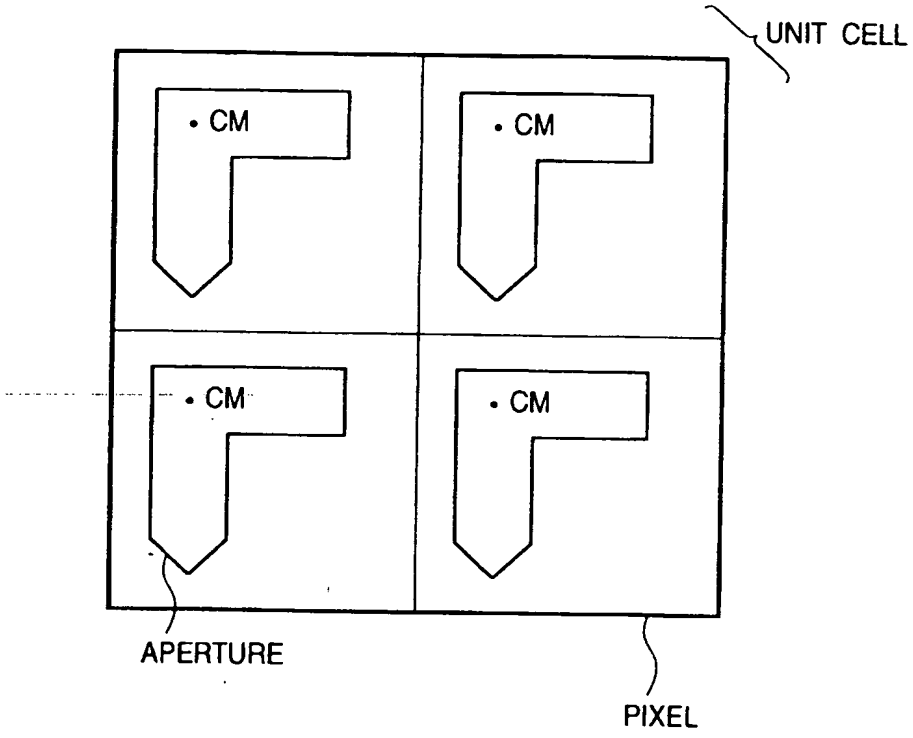


FIG. 28

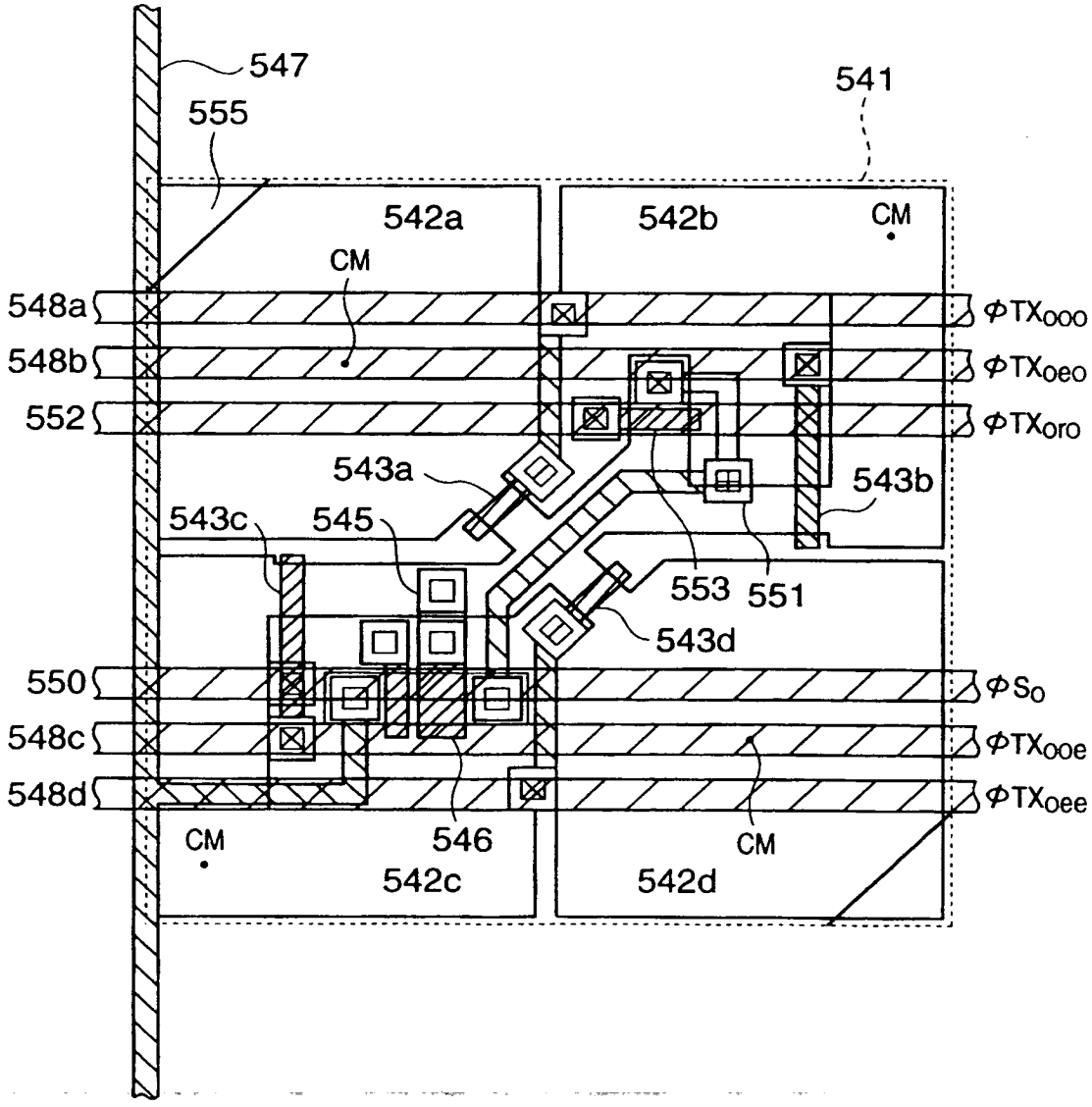


FIG. 29

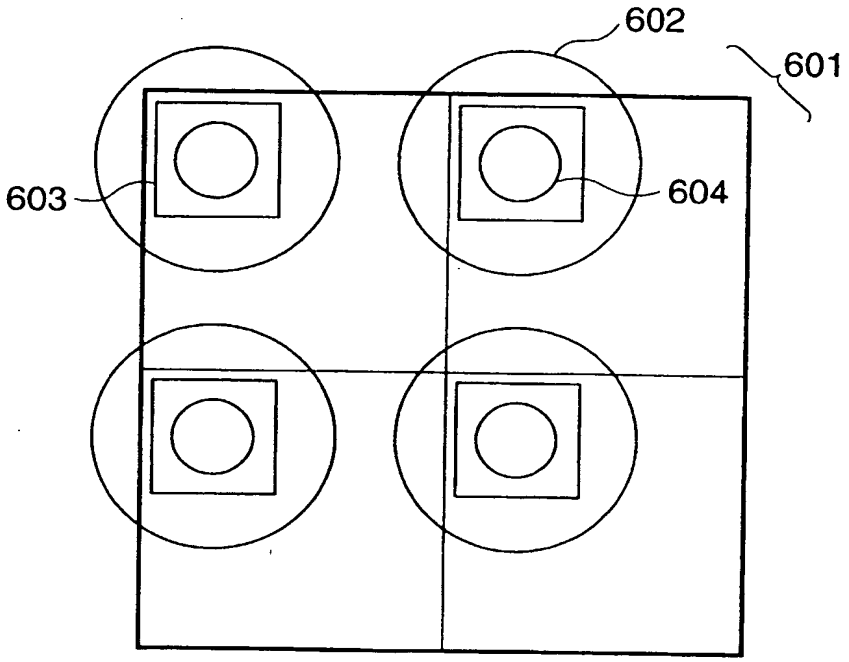


FIG. 30

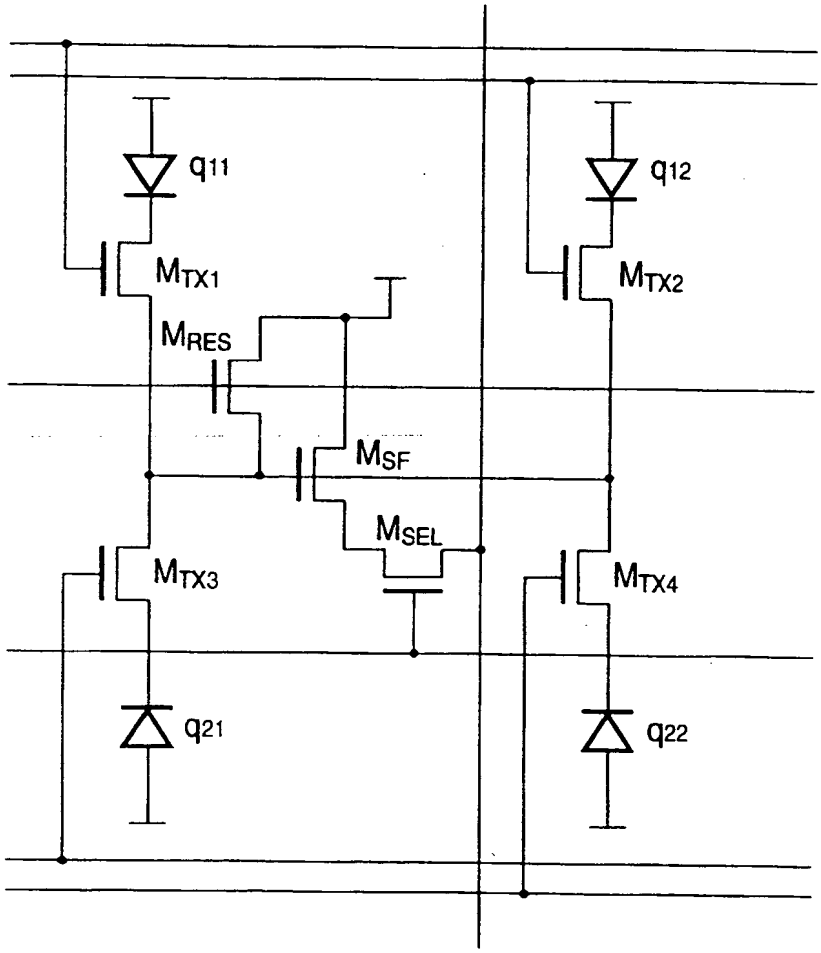


FIG. 31

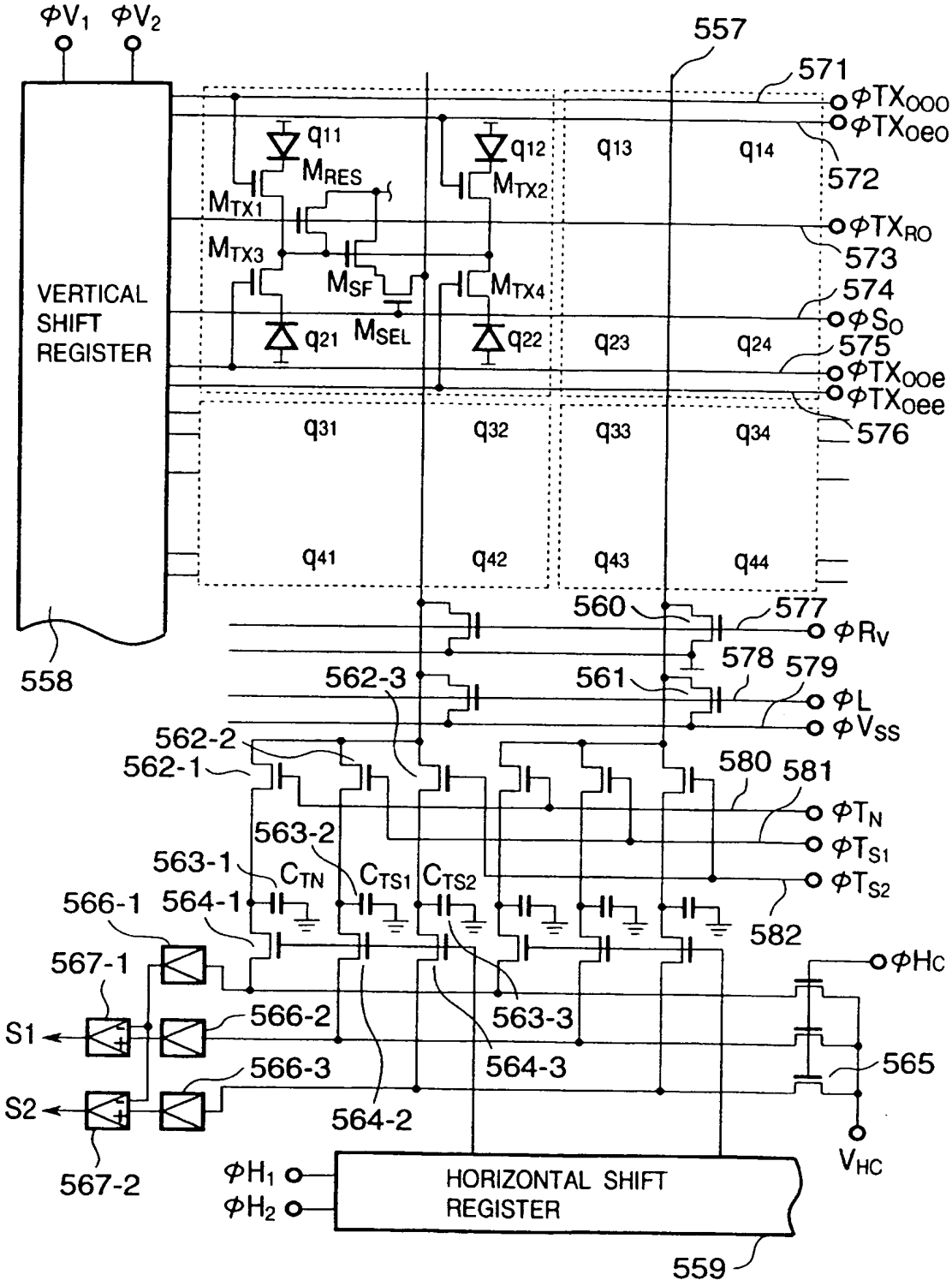


FIG. 32

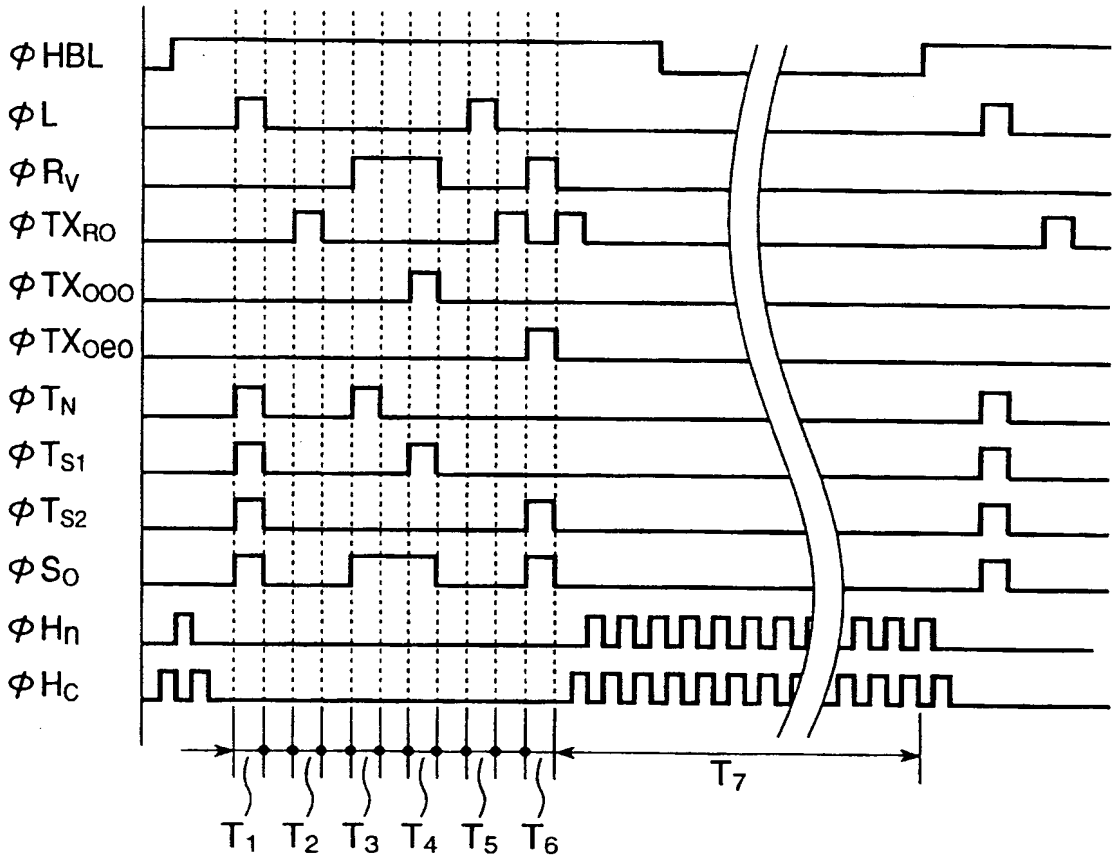


FIG. 33

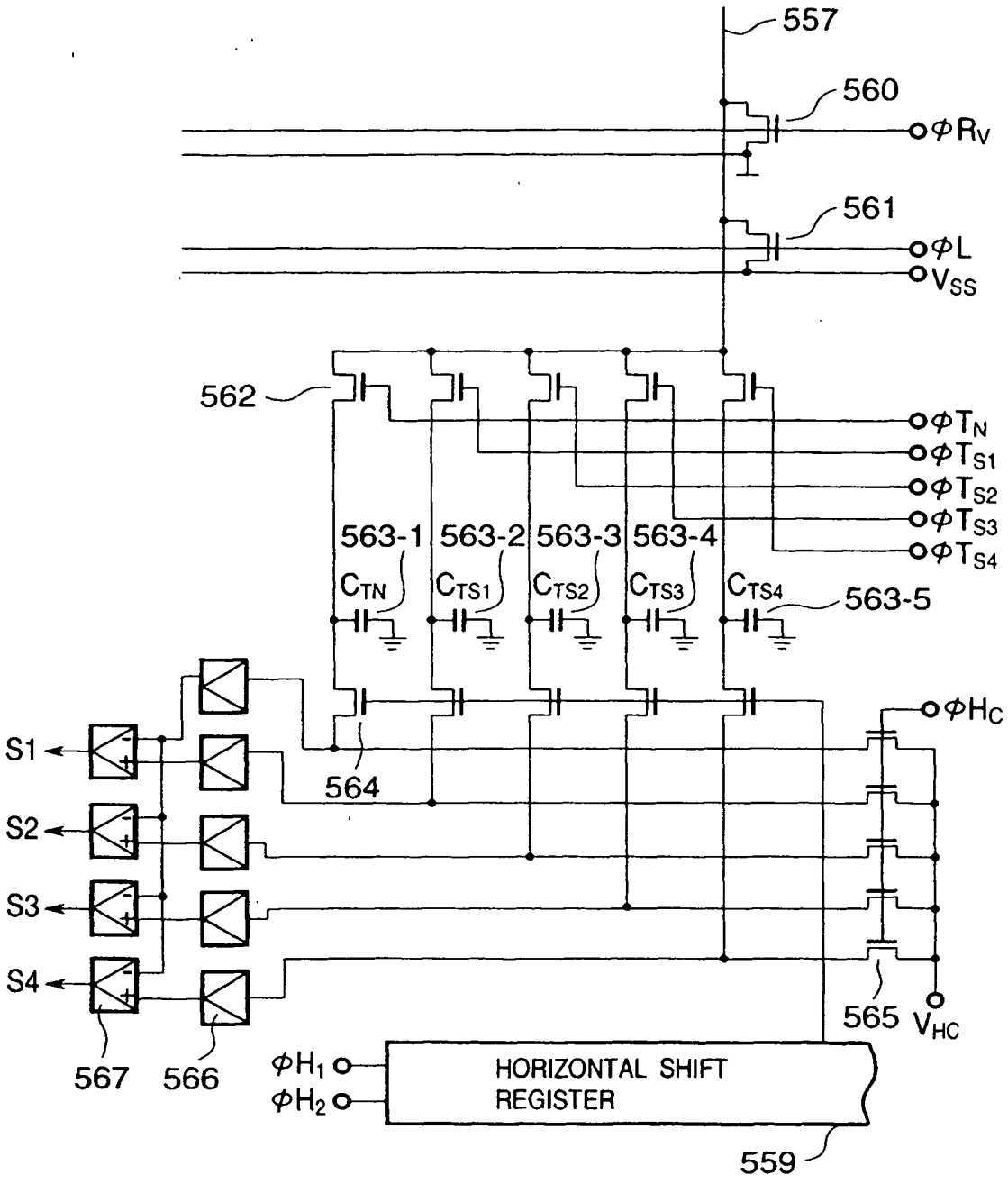


FIG. 34

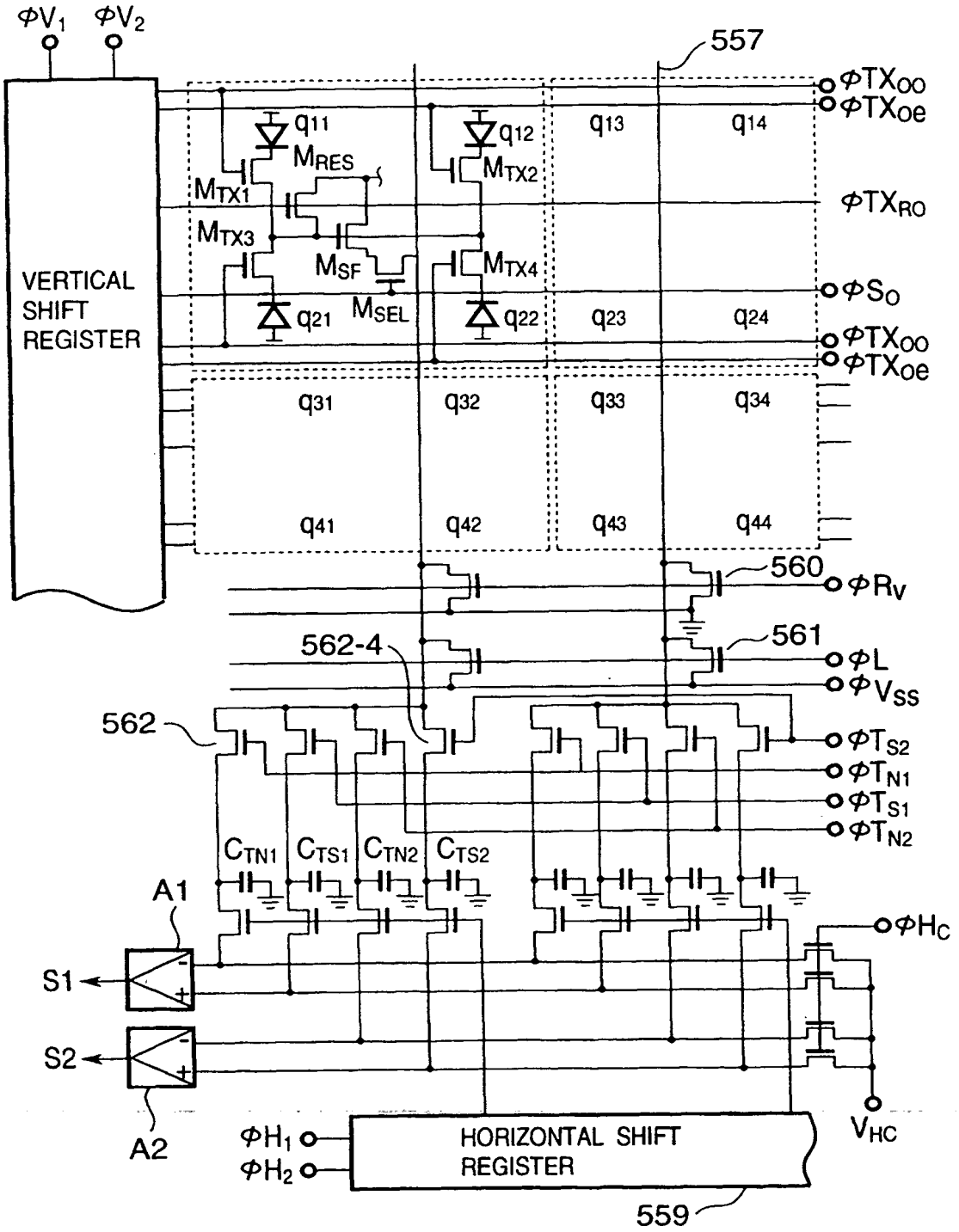


FIG. 35

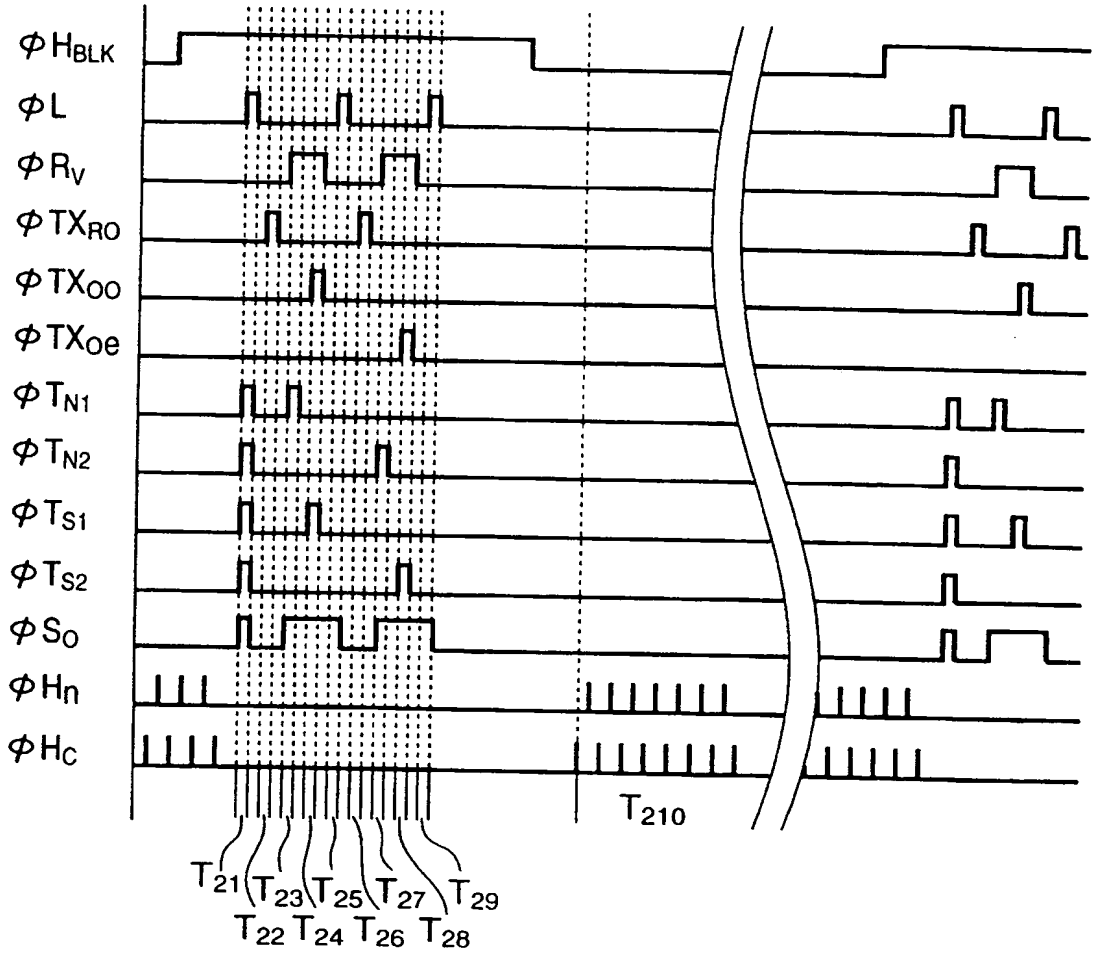


FIG. 36

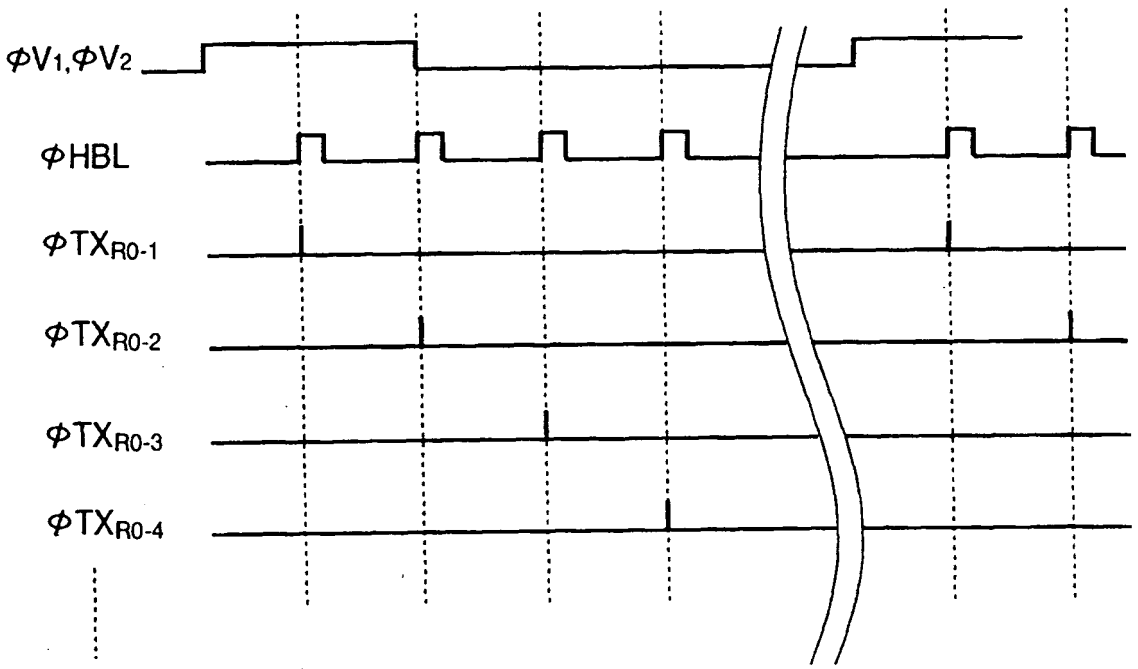


FIG. 37

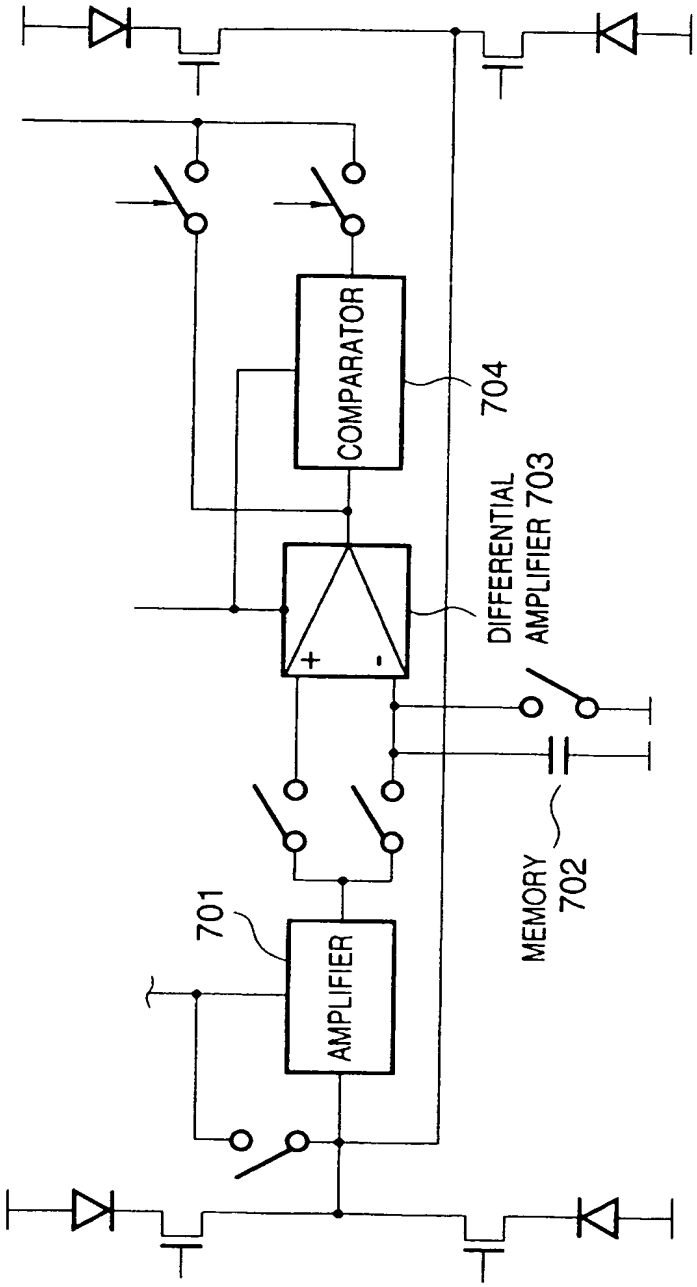


FIG. 38

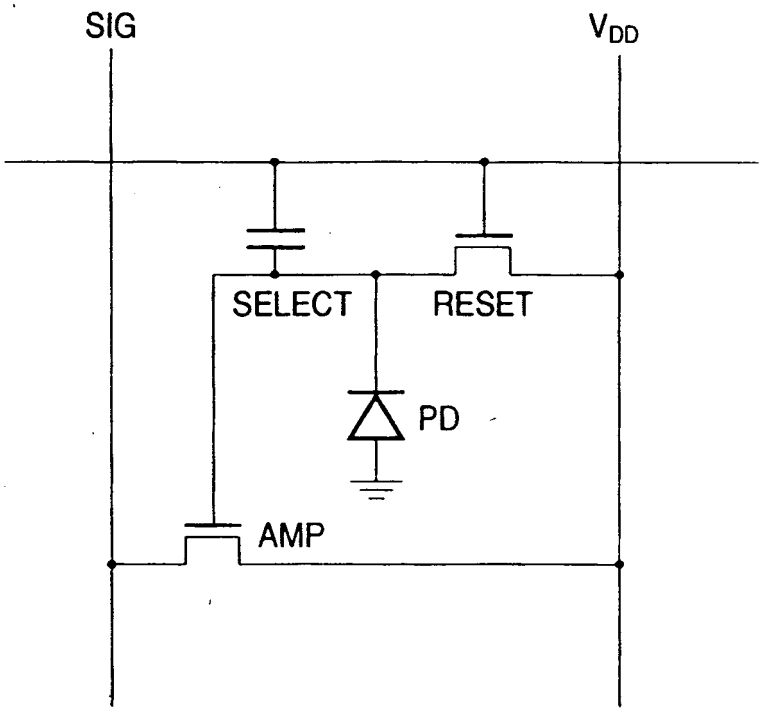


FIG. 39

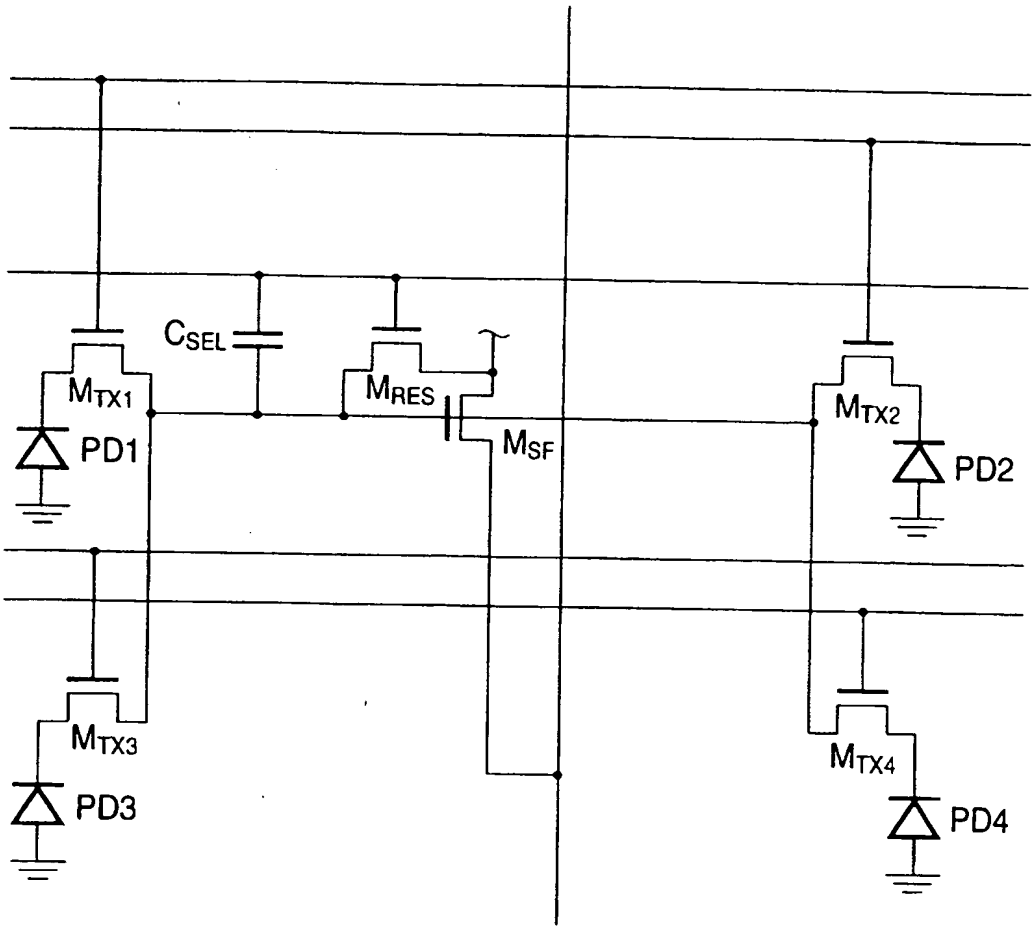


FIG. 40

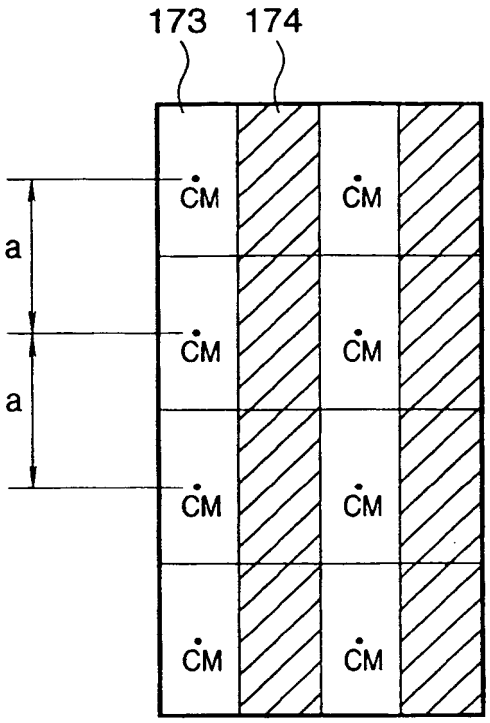


FIG. 41

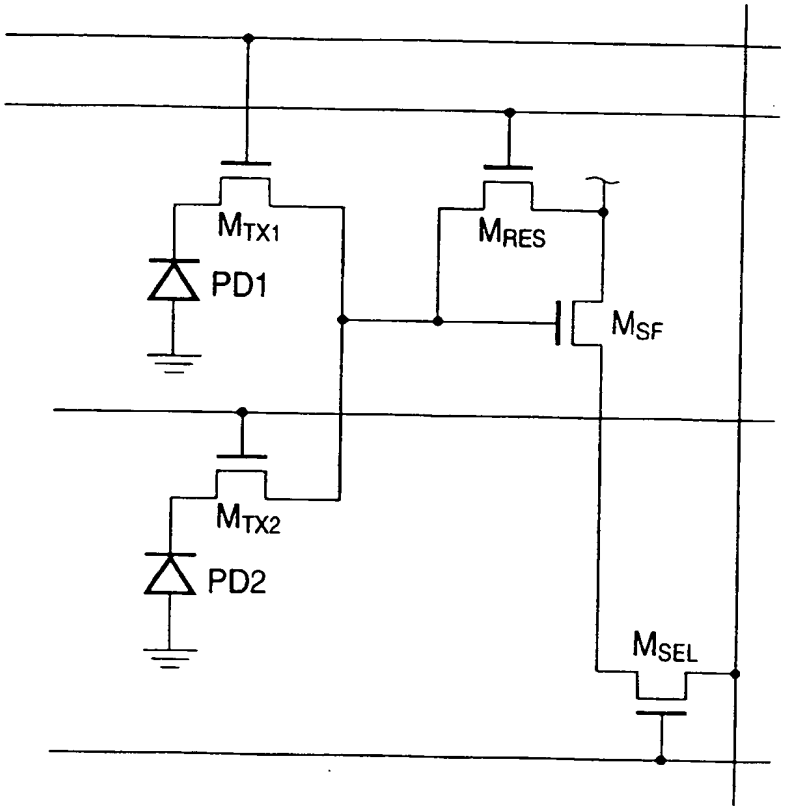


FIG. 42

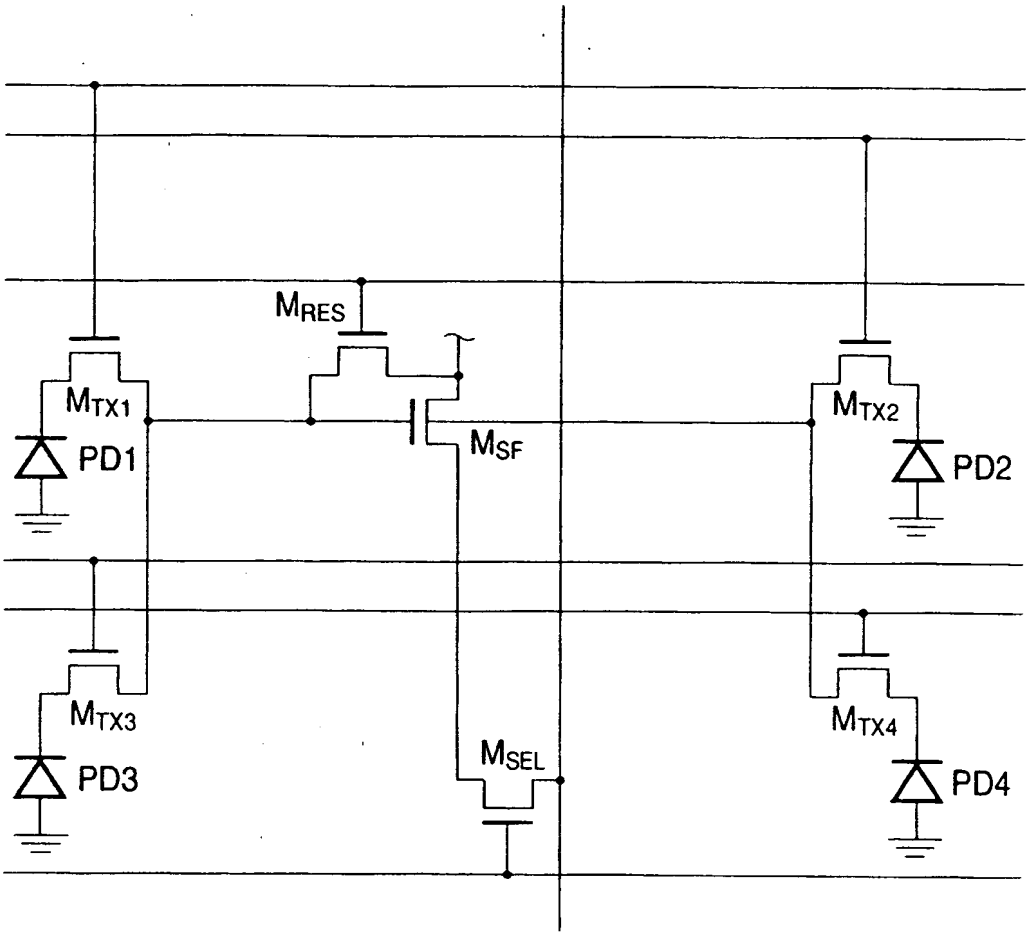


FIG. 43

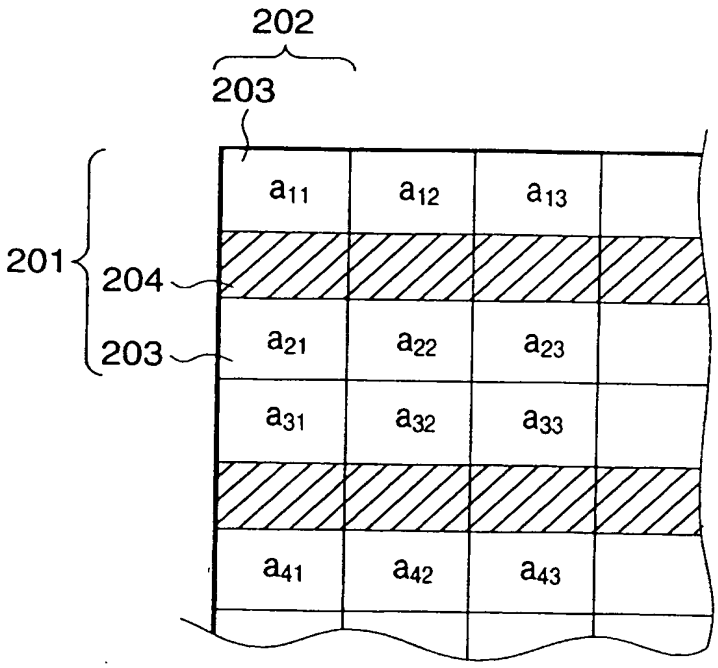


FIG. 44

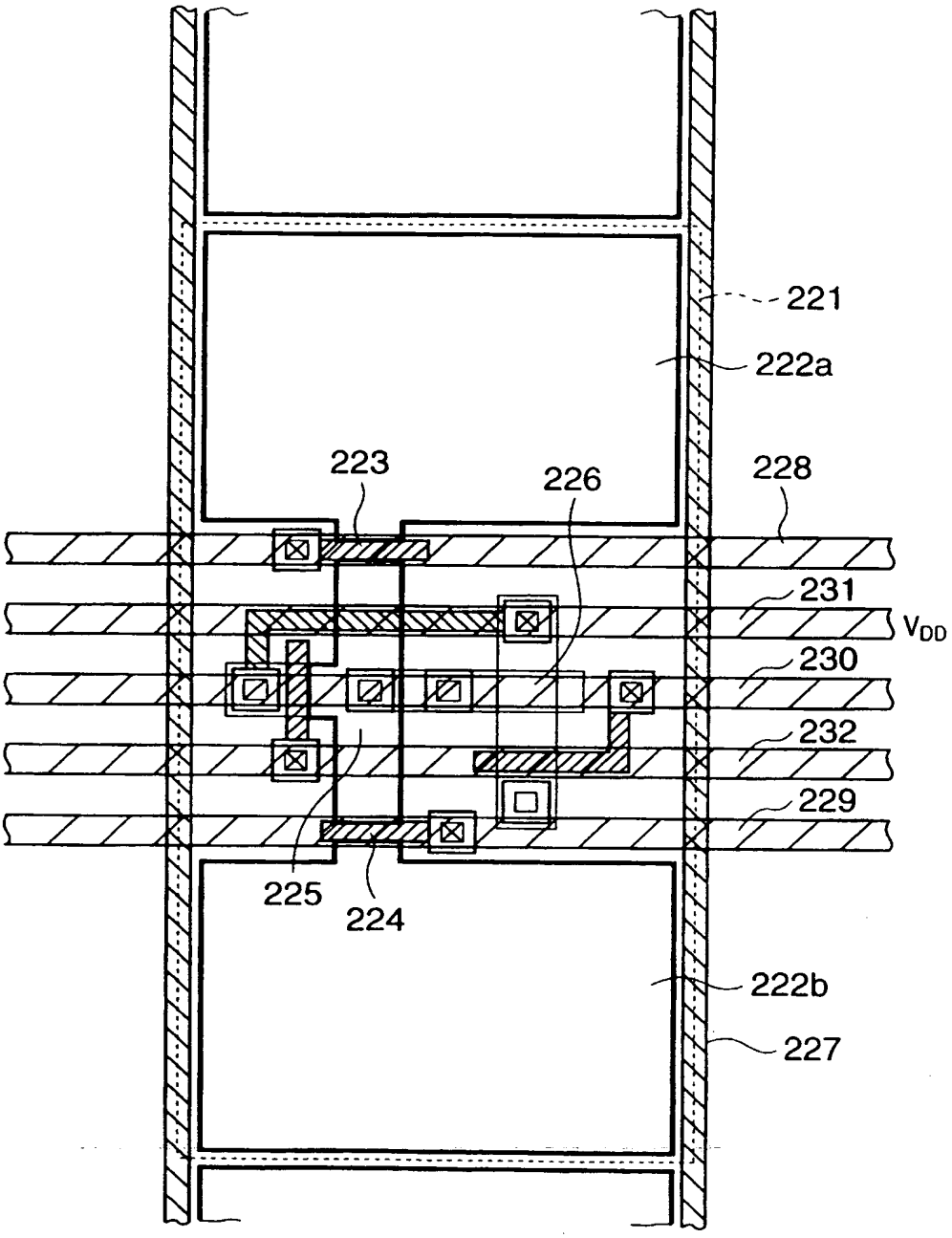


FIG. 45A

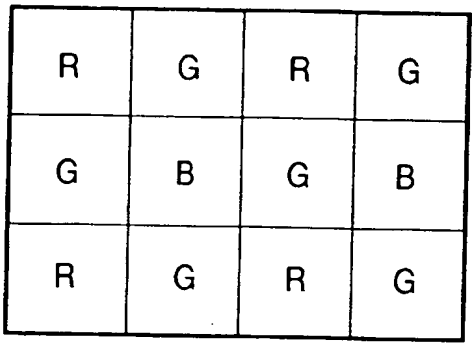


FIG. 45B

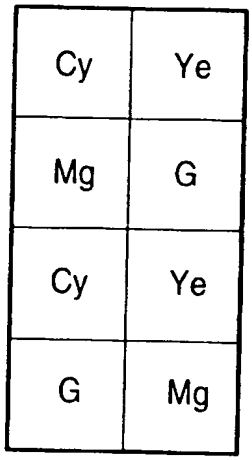
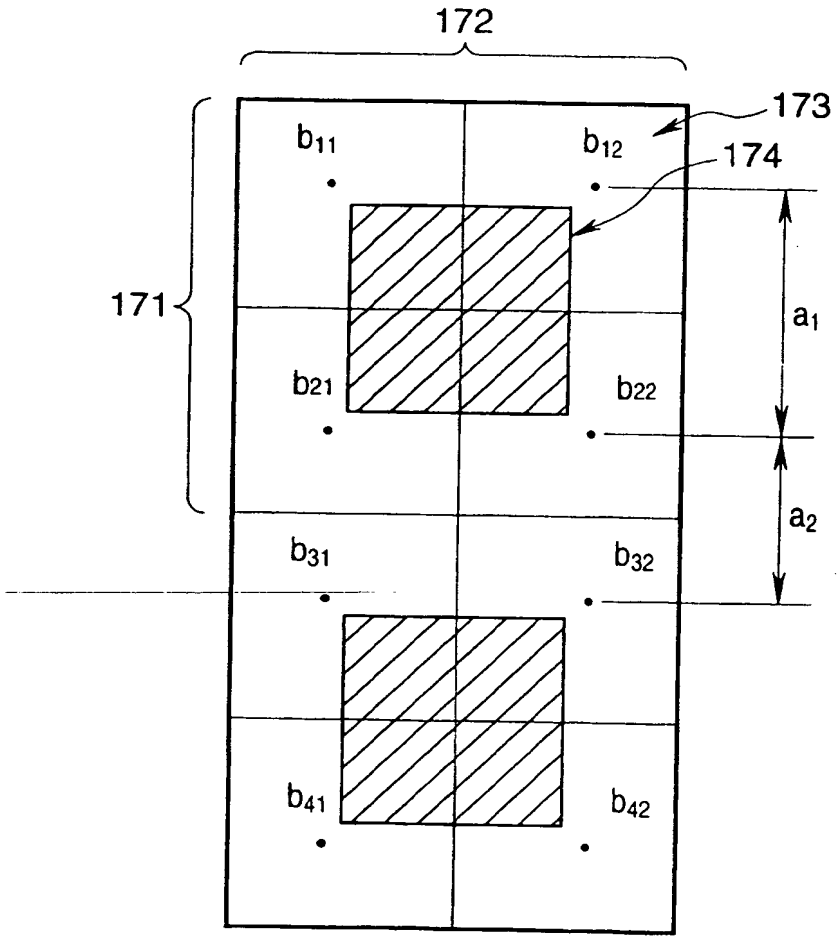
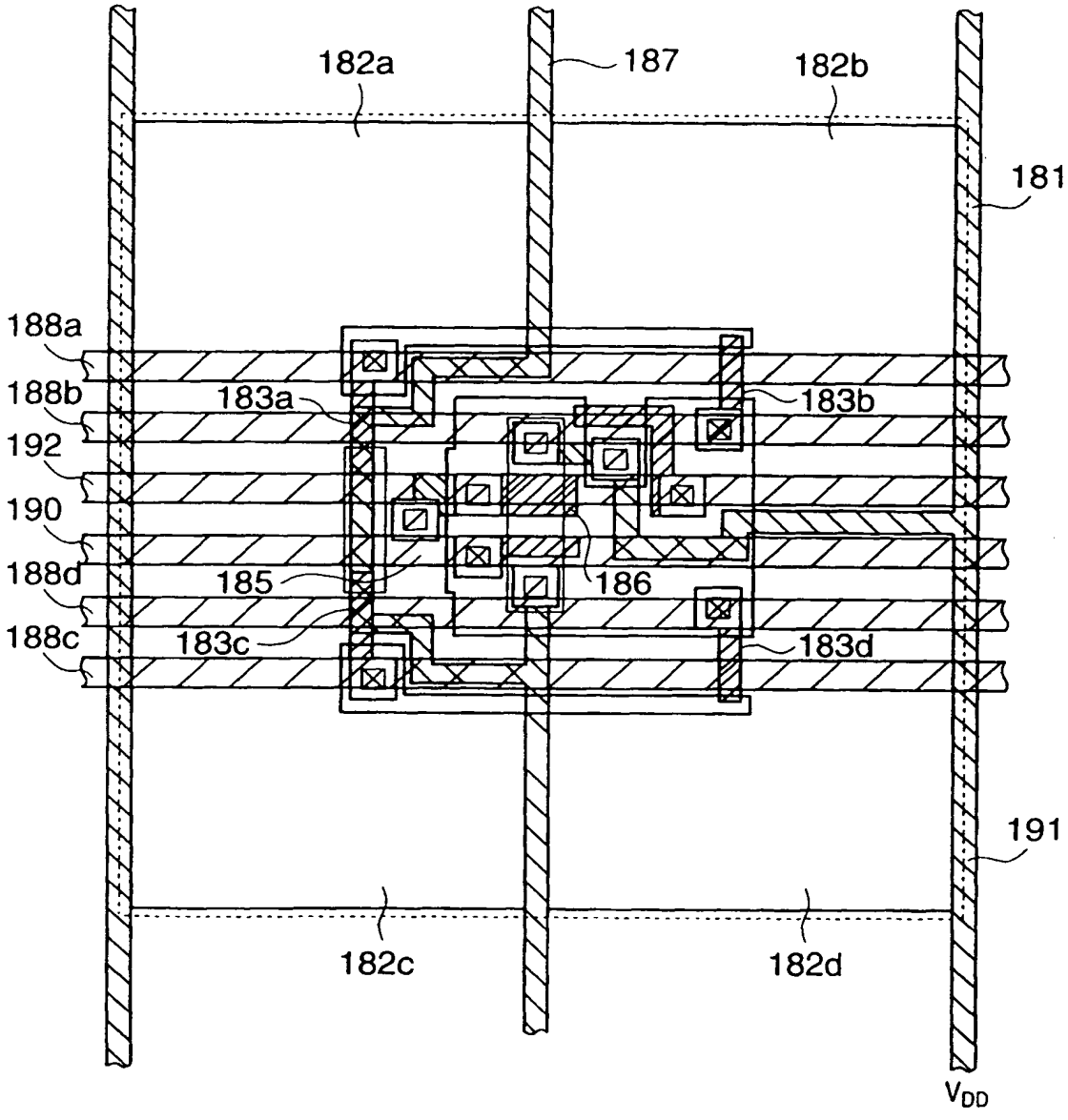


FIG. 46



$a_1 > a > a_2$

FIG. 47



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20.05.1998 JP 13825398
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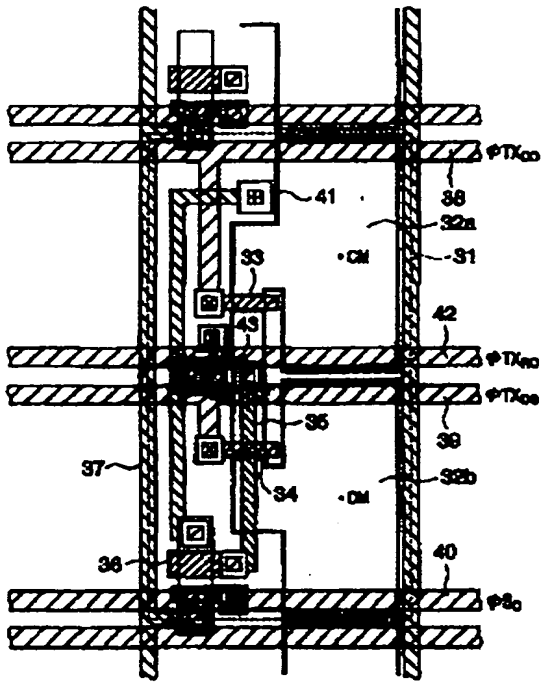
London WC1R 5DJ (GB)

(54) Image sensing apparatus and system including same

(57) In an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, the plurality of photoelectric conversion elements are arranged at a predetermined interval.

FIG. 3



EP 0 954 032 A3

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 3345

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
E,L	EP 0 926 738 A (CANON KK) 30 June 1999 (1999-06-30) * figures 2,4-6 * * column 5, line 51 - column 6, line 48 *	1,2	H01L27/146 H04N3/15
X	US 4 477 835 A (BERGER JEAN L ET AL) 16 October 1984 (1984-10-16) * figures 2-6 * * column 3, line 49 - column 5, line 63 * * column 6, line 8 - column 7, line 41 *	1-3, 14-18, 29-32	
Y		30-32	
Y	PATENT ABSTRACTS OF JAPAN vol. 017, no. 706 (E-1483), 22 December 1993 (1993-12-22) & JP 05 243543 A (NIKON CORP), 21 September 1993 (1993-09-21) * abstract *	30,31	
Y	PATENT ABSTRACTS OF JAPAN vol. 016, no. 316 (E-1231), 10 July 1992 (1992-07-10) -& JP 04 088781 A (CANON INC), 23 March 1992 (1992-03-23) * abstract *	32	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L H04N
X	YAMAWAKI M ET AL: "A PIXEL SIZE SHRINKAGE OF AMPLIFIED MOS IMAGER WITH TWO-LINE MIXING" IEEE TRANSACTIONS ON ELECTRON DEVICES,US,IEEE INC. NEW YORK, vol. 43, no. 5, 1 May 1996 (1996-05-01), pages 713-719, XP000596268 ISSN: 0018-9383 Section III: Device Design * figures 1-4 *	1,3,39, 40,42	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 May 2001	Visscher, E

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 99 30 3345

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☒ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

1-8,14-43

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 3345

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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X,P	EP 0 898 312 A (EASTMAN KODAK CO) 24 February 1999 (1999-02-24) * column 2, line 35 - column 3, line 16 * * figures 2,3 *	1,2,39, 40,42	
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A	HUAT AW CH ET AL: "A 128 X 128-PIXEL STANDARD-CMOS IMAGE SENSOR WITH ELECTRONIC SHUTTER" IEEE JOURNAL OF SOLID-STATE CIRCUITS,US,IEEE INC. NEW YORK, vol. 31, no. 12, 1 December 1996 (1996-12-01), pages 1922-1930, XP000691811 ISSN: 0018-9200 Section III (Circuit design) A: Pixel structure and Circuit * figure 4 *	1,8	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
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This present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 May 2001	Visscher, E

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 99 30 3345

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-8,39-43

   Solid-state imager comprising an one or two dimensional arrangement of pixel-units, which each includes of a number of photosensing elements all sharing a common circuit, wherein:

   said photosensing elements in the pixel-unit are arranged at a predetermined interval and said common circuit constitutes preferential signal-processing circuitry

2. Claims: 9-13

   Solid-state color imager having a two dimensional arrangement of pixel-units, which each includes of a number of photosensing elements sharing a common circuit, wherein:

   each sensor element is provides with a color filter and either neigbouring rows or columns of pixel-units are shifted over a special distance with respect to each other such that the photosensing elements are arranged in a same interval both in the horizontal and vertical direction

3. Claims: 14-32

   Solid-state imager having either a one or two dimensional arrangement of pixel-units, which each includes of a number of photosensing elements all sharing a common circuit, wherein:

   the photosensing elements are provided with a special adjustment means so that the centre of each of the light-receiving areas of the photosensing elements is spaced apart at equal interval

4. Claims: 33-38

   Solid-state imager comprising an one or two dimensional arrangement of pixel-units, which each includes of a number of photosensing elements all sharing a common circuit, wherein:

   said solid-state imager further comprises noise reduction means

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 3345

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 487 (E-1427), 3 September 1993 (1993-09-03) -& JP 05 122440 A (FUJI XEROX CO LTD), 18 May 1993 (1993-05-18) * abstract *	1,29	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 May 2001	Visscher, E

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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L: document cited for other reasons

&: member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 3345

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82